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A Multibus-Compatible 2816 E^2 PROM Memory Board

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INTRODUCTION

The Intel Special Products Division E^2 Multibus Memory Board is an excellent example of how to implement the 2816 Electrically Erasable PROM in a multibus system. The board is completely Multibus compatible and can be plugged into any existing Intellec Microcomputer Development System. It can also be used in a Multibus-compatible system with any combination of Intel Single-Board Computer (iSBC) Modules. The memory board has a capacity of up to 16K bytes of electrically erasable non-volatile memory storage (8 2816s). The board can be read at microprocessor system speeds (250 ns). Writing to the E^2 Board requires only a single system write cycle. When the write operation is complete, the E^2 Board notifies the CPU by lowering an Interrupt Line. Individual 2816s can be erased in a similar manner with one write operation.

The E^2 Memory Board can operate with either an 8 or a 16-bit-wide data bus. This is determined by one jumper and by a 3628A Bipolar PROM used for decoding the addresses to the MOS PROM Array. The 3628A gives the board the capability of accommodating combinations of 2816s, 2815s, 2716s, 2732s, 2732As, and 2764s. The JEDEC pin compatibility of Intel's MOS EPROMs allows these devices to be plugged into the same 28-pin sockets. The 3628A, used as a decoder, allows these different memory size MOS PROMs to be used in the same array in various combinations. This enables the user to mix the devices in the memory array to fit the system's particular applications. The Multibus card can be located anywhere within up to one Megabyte of addressing space. The V_{PP} supply voltage is generated on board, and the only voltages needed are the standard Multibus +5V, +12V, and −12V power supplies. Finally, the E^2 memory system can be powered up and down repeatedly without losing one byte of its 16K bytes of data.

INSTALLATION INSTRUCTIONS

Below is a procedure to prepare the E^2 memory card for use. Following the list are detailed instructions for each step.

Procedure

1. Install the correct shorting plugs on the following jumper groups:

   J9–J12
   Board Address Location

   J13–J19
   RESET and Chip Erase I/O Addresses

   J1–J8
   Interrupt Line Selection

   J20
   Data Bus Width

   J21–J24
   PROM Socket Address Configuration

   JW1–JW8
   PROM/RAM Selection

2. V_{PP} Pulse Width Selection
3. Set switches SW1–SW5 according to the MOS PROM density used.
4. Adjust the V_{PP} high voltage level.
5. Select the proper $\overline{XACK}$ delay based on the t_{ACC} of the slowest MOS PROM used.

Board Address Location

The E^2 board can be assigned to any one of the 16 64K byte pages within a one-megabyte address space. If only 64K of address space is available, leave the jumper pairs J9–J12 open. Otherwise, install the shorting plugs to select the desired page as shown in the following chart:

Board Address Selection

X = install shorting plug
O = open

As shown in the assembly drawing in Appendix D, 2 pins reside at each jumper location. A shorting plug is simply inserted at the jumper location for installation.

64K Page	Jumper			
	J12	J11	J10	J9
0K– 64K	O	O	O	O
64K– 128K	O	O	O	X
128K– 192K	O	O	X	O
192K– 256K	O	O	X	X
256K– 320K	O	X	O	O
320K– 384K	O	X	O	X
384K– 448K	O	X	X	O
448K– 512K	O	X	X	X
512K– 576K	X	O	O	O
576K– 640K	X	O	O	X
640K– 704K	X	O	X	O
704K– 768K	X	O	X	X
768K– 832K	X	X	O	O
832K– 896K	X	X	O	X
896K– 960K	X	X	X	O
960K–1024K	X	X	X	X

RESET and Chip Erase Functions

The board requires two consecutive I/O addresses to control the RESET and Chip Erase functions. Doing an

I/O write cycle to one or the other address activates the particular function. The even I/O address selects the RESET function, an odd I/O address sets the Chip Erase function.

Jumpers J13 through J19 determine which two consecutive I/O addresses are to be used. The following chart shows the jumper scheme for I/O addressing.

	Jumper	J19	J18	J17	J16	J15	J14	J13	
	I/O Address bit	A7	A6	A5	A4	A3	A2	A1	A0
Function	RESET	b	b	b	b	b	b	b	0
	Chip Erase Mode	b	b	b	b	b	b	b	1

b = address bit

Once two consecutive I/O addresses for these two functions are determined, then install shorting plugs on J13–J19 corresponding to the 1's in the upper 7 bits of the two I/O addresses.

Examples:

for 00H = RESET
01H = Chip Erase,
install *no* shorting plugs

for 8AH = RESET
8BH = Chip Erase,
put shorting plugs on J13, J15, and J19

for 32H = RESET
33H = Chip Erase
put shorting plugs on J13, J16, J17

Interrupt Line Selection

The E^2 Memory Board generates an interrupt upon completion of a Byte Erase/Write or a Chip Erase operation. Any one of the 8 Multibus Interrupt Lines can be used. To select a given Interrupt Line, install the shorting plug indicated below:

Interrupt Line	Jumper
$\overline{\text{INT 0}}$	J1
$\overline{\text{INT 1}}$	J2
$\overline{\text{INT 2}}$	J3
$\overline{\text{INT 3}}$	J4
$\overline{\text{INT 4}}$	J5
$\overline{\text{INT 5}}$	J6
$\overline{\text{INT 6}}$	J7
$\overline{\text{INT 7}}$	J8

Data Bus Width

The Multibus Card can use either an 8-bit or a 16-bit-wide data bus. Jumper J20 should be installed for 16-bit data buses, and left open for 8-bit-wide buses.

In addition, switches SW1–SW5 must be set so that the correct MOS PROM(s) are enabled for upper and/or lower byte operations. Refer to the 16-Bit Data Bus Structure section for an explanation of the E^2 Board internal data bus structure. Refer to the following PROM Array Decoder subsection for directions on setting switches SW1–SW5.

PROM/RAM Selection

If E^2PROMs or EPROMs are used in the MOS PROM Array, do the following:

Install shorting plugs on the following jumpers:

JW1, JW3, and JW8

Leave these jumpers OPEN:

JW2, JW4, JW5, JW6, and JW7

V_{PP} PULSE WIDTH SELECTION

Ensure that the correct RC timing components are installed for the E^2PROM to be used:

E^2PROM	R3	C8	t_{WP}
2816	10 KΩ	4.7 μF	10 ms
2815	24 KΩ	10 μF	50 ms

R3 and C8 are located at the top and center of the E^2 board on the left of I.C. H1.

MOS PROM Array Decoder

(See Figure 1) The Bipolar PROM is used to select the MOS PROM or MOS PROM pair being addressed. The Bipolar PROM holds decoding algorithms for 2816s, 2815s, 2716s, 2732s, 2732As, and 2764s. The decoder also selects one or two devices at a time depending on whether an 8-bit or a 16-bit data bus is being used. The Dipswitch at the top of the board determines which decoding algorithm is to be used. Use Table 1 to choose the proper switch setting for the MOS PROMs to be loaded in the Array. The correct shorting plugs must also be installed on Jumpers J21–J24—see Table 2.

If it is desired to have devices of different densities in the Array or if a decoding algorithm other than the one provided is needed, the spare blocks in the 3628A can

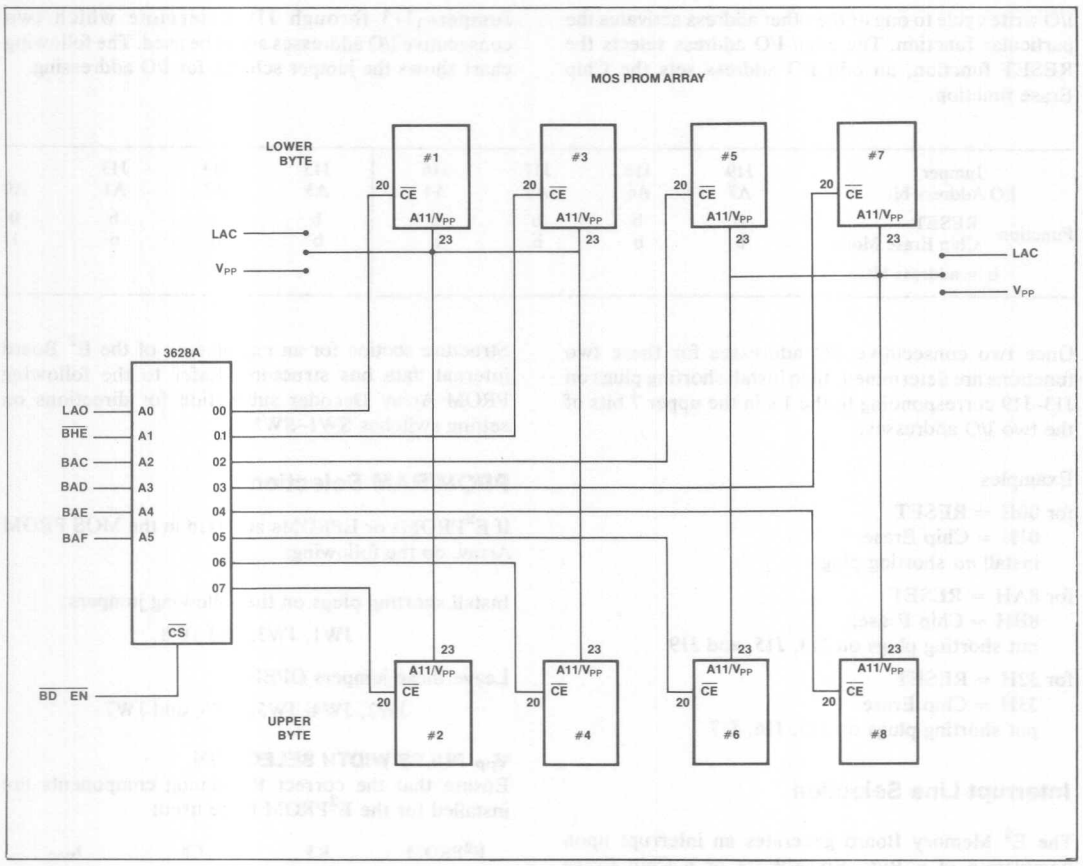


Figure 1. PROM Array Address Configuration

be programmed with new algorithms. The structure of the algorithm is determined by a simple principle. The output corresponding to the $\overline{CE}$ of the MOS PROM to be selected should be a logic 0 for the address range of that PROM. The selecting addresses are A12, A13, A14, A15 (called BAC–BAF on the schematic), and A0 and $\overline{BHE}$. (See section on 16-Bit Data Bus Structure for information on the use of A0 and $\overline{BHE}$.) The smallest address range is 2K bytes. Addresses A12–A15 select a pair of PROMs while A0/$\overline{BHE}$ select one or both of the two PROMs in that pair. Figures 2 through 7 can be used as examples. (Also see Appendix B.)

The decoding algorithms must also take into account the data bus width. See figures 2 through 4 for examples of 8-bit data bus algorithms and figures 5 through 7 for examples of 16-bit data bus algorithms. Note that the proper shorting plugs must be installed on Jumpers J21–J24 according to the device densities used. Jumpers J21–J24 simply connect address A11 or V_{PP} to pin 23 of the 28-pin MOS PROM socket. If a given Array half (sockets 1–4, for example) is to be loaded with 2816s or 2716s, then V_{PP} must go to pin 23 (Jumpers J22 and J24). If 4K or 8K byte parts are used, then All must be connected to pin 23 (Jumpers J21 and J22).

A few rules must be followed in mixed-density Arrays. (1) Each socket pair (1 and 2, 3 and 4, etc.: see Figure 1) must contain devices of the same density. (2) Each Array half (sockets 1–4 and sockets 5–8) can contain either 4K and 8K pairs, or 2K pairs, but not both.

If desired, a 3636B can be used instead of a 3628A. The 2K X 8 3636B will allow the encoding of twice as many decoding algorithms as the 1K X 8 3628A.

The blank PROM Decoder charts in Appendix G may be helpful in planning new decoding algorithms.

SYSTEM ADDRESS A0-15 HEX	DECODER CIRCUIT INPUTS BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	$\overline{CE}$'S 7	6	5	4	3	2	1	0	BYTE
0 X X X	0	0	0	0	1	0							0	0	L
					1	1									H
1 X X X	0	0	0	1	1	0					0	0			L
					1	1									H
2 X X X	0	0	1	0	1	0			0	0					L
					1	1									H
3 X X X	0	0	1	1	1	0	0	0							L
					1	1									H
4 X X X	0	1	0	0	1	0									L
					1	1									H
5 X X X	0	1	0	1	1	0									L
					1	1									H
6 X X X	0	1	1	0	1	0									L
					1	1									H
7 X X X	0	1	1	1	1	0									L
					1	1									H
8 X X X	1	0	0	0	1	0									L
					1	1									H
9 X X X	1	0	0	1	1	0									L
					1	1									H
A X X X	1	0	1	0	1	0									L
					1	1									H
B X X X	1	0	1	1	1	0									L
					1	1									H
C X X X	1	1	0	0	1	0									L
					1	1									H
D X X X	1	1	0	1	1	0									L
					1	1									H
E X X X	1	1	1	0	1	0									L
					1	1									H
F X X X	1	1	1	1	1	0									L
					1	1									H
X=HEX DIGITS	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	
	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

8 BIT DATA BUS

LEAVE JUMPER J20 OPEN. (NO SHORTING PLUG)

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = 2K BYTES

	JUMPERS PROMS: 1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

Figure 2. 2716 or 2816

Table 1. BIP Decoder Switch Settings

Device		2816/2815/2716		2732/2732A	2764
Address Range in Hex (For Full Array)		0000–3FFF	8000–BFFF	0000–7FFF	0000–FFFF
8-Bit Data Bus	SW1	ON	ON	OFF	ON
	SW2	ON	OFF	OFF	OFF
	SW3	ON	OFF	ON	ON
	SW4	ON	ON	ON	ON
	*SW5	ON	ON	ON	ON
16-Bit Data Bus	SW1	OFF	OFF	ON	OFF
	SW2	OFF	OFF	ON	ON
	SW3	ON	OFF	OFF	OFF
	SW4	ON	ON	ON	ON
	*SW5	ON	ON	ON	ON

OFF = No shorting plug.
ON = Install shorting plug.
*Must Be "ON" for 3628A.

SYSTEM ADDRESS A0-15 HEX	DECODER CIRCUIT INPUTS BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	$\overline{CE}$'S 7	6	5	4	3	2	1	0	BYTE
0 X X X	0	0	0	0	1	0							0	0	L
					1	1									H
1 X X X	0	0	0	1	1	0							0	0	L
					1	1									H
2 X X X	0	0	1	0	1	0					0	0			L
					1	1									H
3 X X X	0	0	1	1	1	0					0	0			L
					1	1									H
4 X X X	0	1	0	0	1	0			0	0					L
					1	1									H
5 X X X	0	1	0	1	1	0			0	0					L
					1	1									H
6 X X X	0	1	1	0	1	0	0	0							L
					1	1									H
7 X X X	0	1	1	1	1	0	0	0							L
					1	1									H
8 X X X	1	0	0	0	1	0									L
					1	1									H
9 X X X	1	0	0	1	1	0									L
					1	1									H
A X X X	1	0	1	0	1	0									L
					1	1									H
B X X X	1	0	1	1	1	0									L
					1	1									H
C X X X	1	1	0	0	1	0									L
					1	1									H
D X X X	1	1	0	1	1	0									L
					1	1									H
E X X X	1	1	1	0	1	0									L
					1	1									H
F X X X	1	1	1	1	1	0									L
					1	1									H
X=HEX DIGITS	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	
	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

8 BIT DATA BUS

LEAVE JUMPER J20 OPEN. (NO SHORTING PLUG)

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = 4K BYTES

	JUMPERS			
PROMS:	1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

Figure 3. 2732 or 2732A

Table 2. MOS PROM Sockets

Device Density	1–4		5–8	
	J21	J22	J23	J24
2K	O	X	O	X
4K or 8K	X	O	X	O

O = No shorting plug.
X = Install shorting plug.

SYSTEM ADDRESS A0-15 HEX	DECODER CIRCUIT INPUTS						CE'S								BYTE
	BAF	BAE	BAD	BAC	BHEN	LA0	7	6	5	4	3	2	1	0	
0 X X X	0	0	0	0	1	0							0		L
					1	1								0	H
1 X X X	0	0	0	1	1	0							0		L
					1	1								0	H
2 X X X	0	0	1	0	1	0							0		L
					1	1								0	H
3 X X X	0	0	1	1	1	0							0		L
					1	1								0	H
4 X X X	0	1	0	0	1	0					0	0			L
					1	1					0				H
5 X X X	0	1	0	1	1	0					0	0			L
					1	1					0				H
6 X X X	0	1	1	0	1	0					0	0			L
					1	1					0				H
7 X X X	0	1	1	1	1	0					0	0			L
					1	1					0				H
8 X X X	1	0	0	0	1	0			0	0					L
					1	1			0						H
9 X X X	1	0	0	1	1	0			0	0					L
					1	1			0						H
A X X X	1	0	1	0	1	0			0	0					L
					1	1			0						H
B X X X	1	0	1	1	1	0			0	0					L
					1	1			0						H
C X X X	1	1	0	0	1	0	0	0							L
					1	1	0								H
D X X X	1	1	0	1	1	0	0	0							L
					1	1	0								H
E X X X	1	1	1	0	1	0	0	0							L
					1	1	0								H
F X X X	1	1	1	1	1	0	0	0							L
					1	1	0								H
X=HEX DIGITS	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	
	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

8 BIT DATA BUS

LEAVE JUMPER J20 OPEN. (NO SHORTING PLUG)

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = 8K BYTES

	JUMPERS			
PROMS:	1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

Figure 4. 2764

SYSTEM ADDRESS A0–15 HEX	DECODER CIRCUIT INPUTS						$\overline{CE}$'S								BYTE
	BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	7	6	5	4	3	2	1	0	
0XXX	0	0	0	0	0	0							0	0	W
					1	0							0	0	L
					0	1									H
1XXX	0	0	0	1	0	0					0	0			W
					1	0					0	0			L
					0	1									H
2XXX	0	0	1	0	0	0			0	0					W
					1	0			0	0					L
					0	1									H
3XXX	0	0	1	1	0	0	0	0							W
					1	0	0	0							L
					0	1									H
4XXX	0	1	0	0	0	0									W
					1	0									L
					0	1									H
5XXX	0	1	0	1	0	0									W
					1	0									L
					0	1									H
6XXX	0	1	1	0	0	0									W
					1	0									L
					0	1									H
7XXX	0	1	1	1	0	0									W
					1	0									L
					0	1									H
8XXX	1	0	0	0	0	0									W
					1	0									L
					0	1									H
9XXX	1	0	0	1	0	0									W
					1	0									L
					0	1									H
AXXX	1	0	1	0	0	0									W
					1	0									L
					0	1									H
BXXX	1	0	1	1	0	0									W
					1	0									L
					0	1									H
CXXX	1	1	0	0	0	0									W
					1	0									L
					0	1									H
DXXX	1	1	0	1	0	0									W
					1	0									L
					0	1									H
EXXX	1	1	1	0	0	0									W
					1	0									L
					0	1									H
FXXX	1	1	1	1	0	0									W
					1	0									L
					0	1									H
	A5	A4	A3	A2	A1	A0	07	06	05	04	03	02	01	00	
X = HEX DIGITS	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

16 BIT DATA BUS

INSTALL SHORTING PLUG AT JUMPER J20.

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = 2K BYTES

	JUMPERS			
	PROMS: 1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

Figure 5. 2716 or 2816

SYSTEM ADDRESS A0–15 HEX	DECODER CIRCUIT INPUTS						$\overline{CE}$'S								BYTE
	BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	7	6	5	4	3	2	1	0	
0XXX	0	0	0	0	0 1 0	0 0 1							0 0	0 0	W L H
1XXX	0	0	0	1	0 1 0	0 0 1							0 0	0 0	W L H
2XXX	0	0	1	0	0 1 0	0 0 1					0 0	0 0			W L H
3XXX	0	0	1	1	0 1 0	0 0 1					0 0	0 0			W L H
4XXX	0	1	0	0	0 1 0	0 0 1			0 0	0 0					W L H
5XXX	0	1	0	1	0 1 0	0 0 1			0 0	0 0					W L H
6XXX	0	1	1	0	0 1 0	0 0 1	0 0	0 0							W L H
7XXX	0	1	1	1	0 1 0	0 0 1	0 0	0 0							W L H
8XXX	1	0	0	0	0 1 0	0 0 1									W L H
9XXX	1	0	0	1	0 1 0	0 0 1									W L H
AXXX	1	0	1	0	0 1 0	0 0 1									W L H
BXXX	1	0	1	1	0 1 0	0 0 1									W L H
CXXX	1	1	0	0	0 1 0	0 0 1									W L H
DXXX	1	1	0	1	0 1 0	0 0 1									W L H
EXXX	1	1	1	0	0 1 0	0 0 1									W L H
FXXX	1	1	1	1	0 1 0	0 0 1									W L H
	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	
X = HEX DIGITS	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

16 BIT DATA BUS

INSTALL SHORTING PLUG AT JUMPER J20.

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = 4K BYTES

	JUMPERS			
	PROMS: 1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

Figure 6. 2732 or 2732A

SYSTEM ADDRESS A0–15 HEX	DECODER CIRCUIT INPUTS						$\overline{CE}$'S								BYTE
	BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	7	6	5	4	3	2	1	0	
0 X X X	0	0	0	0	0 1 0	0 0 1							0 0	0 0	W L H
1 X X X	0	0	0	1	0 1 0	0 0 1							0 0	0 0	W L H
2 X X X	0	0	1	0	0 1 0	0 0 1							0 0	0 0	W L H
3 X X X	0	0	1	1	0 1 0	0 0 1							0 0	0 0	W L H
4 X X X	0	1	0	0	0 1 0	0 0 1					0 0	0 0			W L H
5 X X X	0	1	0	1	0 1 0	0 0 1					0 0	0 0			W L H
6 X X X	0	1	1	0	0 1 0	0 0 1					0 0	0 0			W L H
7 X X X	0	1	1	1	0 1 0	0 0 1					0 0	0 0			W L H
8 X X X	1	0	0	0	0 1 0	0 0 1			0 0	0 0					W L H
9 X X X	1	0	0	1	0 1 0	0 0 1			0 0	0 0					W L H
A X X X	1	0	1	0	0 1 0	0 0 1			0 0	0 0					W L H
B X X X	1	0	1	1	0 1 0	0 0 1			0 0	0 0					W L H
C X X X	1	1	0	0	0 1 0	0 0 1	0 0	0 0							W L H
D X X X	1	1	0	1	0 1 0	0 0 1	0 0	0 0							W L H
E X X X	1	1	1	0	0 1 0	0 0 1	0 0	0 0							W L H
F X X X	1	1	1	1	0 1 0	0 0 1	0 0	0 0							W L H
	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	

X = HEX DIGITS

ADDRESS INPUTS 3628A

OUTPUTS

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

16 BIT DATA BUS

INSTALL SHORTING PLUG AT JUMPER J20.

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = 8K BYTES

	JUMPERS			
PROMS:	1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

Figure 7. 2764

Adjusting the V_{PP} Voltage Level

The high level of the V_{PP} pulse must be calibrated to 21V. The 8085A code sequence shown below or an equivalent write routine can be used to generate a series of V_{PP} pulses for initial calibration purposes.

```
        MVI A,
        COUNT       ; COUNT = number required for
                      delay of at least 40 ms.
        OUT 0       ; RESET the board
WRTLP:
        STA 8000H   ; send a write command to the E2
                      Memory board
        LXI B, 0
DLYLP:
        INX B
        CMP B       ; compare B reg with Count
        JNZ DLYLP   ; done yet?
        OUT 0       ; Yes, RESET board and start again
        JMP WRTLP
```

The oscilloscope used should first be calibrated against a known 21.0V DC source. For the above program loop, the board address is 8000H and the RESET I/O address 00H. Remove the shorting plugs from J9-J12. Set switches SW 1-5 to on, off, off, on, on, respectively. Before running any V_{PP} pulse loop on the E^2 Board,

1. Remove all shorting plugs from jumpers J1-J8
2. Remove *all 2816's* from the board. Otherwise the maximum write cycle capacity at the addressed 2816 could be exceeded and the useful device life could be diminished.

$\overline{\text{XACK}}$ Delay

To select R7 use the following table and the tacc value of the slowest device in the PROM Array:

tacc (ns)	XACL delay (ns)	R7 (ohms)
200	250	6K
250	300	7.5K
350	400	12K
450	500	15K
650	700	24K

USER'S OPERATIONAL INSTRUCTIONS

The Multibus Board can be read by simply sending a Memory Read command to the board.

A byte or word write is performed on the system by doing a normal Memory Write Cycle. The Bus CPU will be informed approximately 25ms later via an Interrupt Line that the E^2 Board has completed the write operation. The CPU clears the Interrupt by RESETING the E^2 Board. The board is then ready for a new command.

Each 2816 E^2PROM on the E^2 Board can be erased with one write operation. To accomplish this, the board is first put into Chip Erase Mode by doing an I/O Write cycle to the Chip Erase I/O address. The data written during the I/O Write cycle is not used by the E^2 Board. A Memory Write cycle is then performed on the 2816 to be erased. As with the data write cycle described above, an Interrupt Line will be lowered when the Chip Erase operation has been completed. The CPU issues a RESET to the E^2 Board by doing an I/O Write cycle to the RESET I/O address. (The data put on the system bus during the RESET I/O write cycle is not used.) The 2816 that was written now contains all 1's, the Chip Erase Mode is cleared, and the E^2 Board is ready for the next command.

After powering up the E^2 Memory Board, the CPU must send an initial RESET to the E^2 Board to prepare it for normal operation. This should not occur until the CPU has been running for at least 1 second.

E^2 Memory Board Operation Summary

Operation	CPU Action	E^2 Board Action	Comments
Read	Memory Read command $\overline{MRDC}$	data requested is put on the bus	Minimum delay from $\overline{MRDC}$ to $\overline{XACK}$ = 250 ns
Write	Memory Write command $\overline{MWTC}$		byte or word erase and byte or word write is performed on 2816 or 2816 pair
		an $\overline{INT}$ line is pulled low when operation is done	
	issue RESET		
Chip Erase	Set Chip Erase Mode with an I/O Write Command—then send an $\overline{MWTC}$ to the one or two 2816's to be erased		One or two 2816's are set to all 1's
		$\overline{INT}$ goes low when done	
	issue RESET		
Initialize E^2 Board	After the CPU starts running, wait 1 second, then send RESET command.		E^2 Board is ready for operation

USER PROGRAM EXAMPLE

This sample program transfers a block of data from a RAM buffer to the E^2 memory on the E^2 Memory Board. The system data bus is 8-bits wide, and the RAM memory block is located from 0 to 64K. (The Memory Board is located from 8000H to BFFFH. The system RAM is inhibited by $\overline{INH1}$ from the E^2 Board whenever the latter is accessed.) All 8 MOS PROM sockets are loaded with 2816's. The I/O addresses are 00H for RESET and 01H for Chip Erase Mode. The data transfer in this example consists of less than 4K bytes. The transfer is started by doing an initial Memory Write Cycle to the E^2 Board. Following the Write Cycle, the interrupt subroutine (SRVINT) RESET's the E^2 Board after each write operation has been completed. The subroutine will then take the next data byte from the RAM source block and write it to the next E^2 location. At this point, the subroutine returns control to the main program which in this example idles in a tight loop. An actual system CPU would continue doing its main processing until the present write operation was done. Once the data transfer is started, the interrupt subroutine will take care of reseting the E^2 Board and writing the next byte. The subroutine takes only about 100 μs out of every 20 ms of CPU time to carry out the data transfer. The data transfer is thus highly efficient.

```
LOC  OBJ        LINE       SOURCE STATEMENT

                    1 ;
                    2 ;
                    3 ;*****************************************************************
                    4 ;
                    5 ;
                    6 ;          INTEL CORPORATION
                    7 ;
                    8 ;          SPD E2 MULTIBUS COMPATIBLE MEMORY BOARD
                    9 ;
                   10 ;          APPLICATION PROGRAM
                   11 ;
                   12 ;
                   13 ;
                   14 ;
                   15 ;*****************************************************************
                   16 ;
                   17 ;
                   18 ;
                   19 ;
                   20 ;     THIS PROGRAM DOES A DATA TRANSFER
                   21 ;     BETWEEN A BLOCK OF RAM AND THE E2
                   22 ;     MEMORY BOARD
                   23 ;
                   24 ;     THE RAM BLOCK IS LOCATED AT 0C000H
                   25 ;
                   26 ;     THE E2 BOARD IS LOCATED AT ADDRESS 8000H
                   27 ;
                   28 ;     IO ADDRESSES:
                   29 ;          00H - RESET
                   30 ;          01H - CHIP ERASE
                   31 ;
                   32 ;     INTERRUPT LINE 7 (INT7') IS USED TO INFORM
                   33 ;     THE CPU WHEN THE E2 BOARD HAS COMPLETED A
                   34 ;     BYTE ERASE/WRITE OR A CHIP ERASE COMMAND
                   35 ;
                   36 ;     0E00H DATA BYTES ARE TRANSFERRED
                   37 ;
                   38 ;
                   39 ;
                   40 ;
                   41 ;
8000               42 STRADD          EQU     8000H
00FC               43 INTMSK          EQU     0FCH
00FD               44 OLRSTR          EQU     0FDH
000D               45 CR              EQU     0DH
000A               46 LF              EQU     0AH
0009               47 EXIT            EQU     9
                   48 ;
                   49                 EXTRN   CO,CI,ISIS
                   50 ;
                   51 ;
                   52 ;
7800               53                 ORG     7800H
                   54 ;
```

```
LOC  OBJ          LINE       SOURCE STATEMENT

7800 C34678         55         JMP     INIT
                    56 ;
                    57 ;
                    58 ;
                    59 ;   ************************************************
                    60 ;
                    61 ;
                    62 ;
                    63 ;          DATA STRINGS
                    64 ;
                    65 ;
                    66 ;************************************************
                    67 ;
                    68 ;
7803 5452414E       69 TRNMSG:          DB      'TRANSFER IN PROGRESS',CR,LF,0FFH
7807 53464552
780B 20494E20
780F 50524F47
7813 52455353
7817 0D
7818 0A
7819 FF
781A 44415441       70 ERRMSG:          DB      'DATA ERROR',CR,LF,0FFH
781E 20455252
7822 4F52
7824 0D
7825 0A
7826 FF
7827 5452414E       71 FINMSG:          DB      'TRANSFER COMPLETE',CR,LF,0FFH
782B 53464552
782F 20434F4D
7833 504C4554
7837 45
7838 0D
7839 0A
783A FF
783B 3D78           72 EBLK:            DW      ESTAT
                    73 ;
                    74 ;
                    75 ;
                    76 ;****************************************
                    77 ;
                    78 ;
                    79 ;     TEMPORARY STORAGE SPACE
                    80 ;
                    81 ;
                    82 ;****************************************
                    83 ;
                    84 ;
783D                85 ESTAT:           DS      2
783F                86 E2BUSY:          DS      1
7840                87 MSGADD:          DS      2
7842                88 SRCADD:          DS      2
7844                89 DESADD:          DS      2
                    90 ;
```

```
LOC  OBJ        LINE       SOURCE STATEMENT

                  91 ;
                  92 ;
                  93 ;
                  94 INIT:
7846 31007E       95         LXI     SP,7E00H
7849 D300         96         OUT     0                ;RESET THE E2 BOARD
                  97 ;
                  98 ;
                  99 ;     LOAD LOCATION 038H(INTERRUPT 7 VECTOR)
                 100 ;     WITH JUMP TO SERVICE INTERRUPT SUBROUTINE
                 101 ;
784B 3EC3        102         MVI     A,0C3H
784D 323800      103         STA     38H
7850 21AE78      104         LXI     H,SRVINT
7853 223900      105         SHLD    39H
                 106 ;
                 107 ;     SET THE SYSTEM INTERRUPT MASK TO
                 108 ;     ENABLE INTERRUPTS 1 AND 7
                 109 ;
                 110 ;
                 111 ;
7856 3E7E        112         MVI     A,7EH
7858 D3FC        113         OUT     INTMSK
785A FB          114         EI
785B 210378      115         LXI     H,TRNMSG              ;INFORM OPERATOR
                 116                                       ;THAT THE TRANSFER
                 117                                       ;HAS BEGUN
                 118 ;
785E 224078      119         SHLD    MSGADD
7861 CDE578      120         CALL    DISMSG
                 121 ;
                 122 ;
                 123 ;
                 124 ;**************************
                 125 ;
                 126 ;     MAIN PROGRAM
                 127 ;
                 128 ;
                 129 MAINPG:
                 130 ;
                 131 ;     LOAD SOURCE RAM BLOCK WITH 55H
                 132 ;
7864 2100C0      133         LXI     H,RAMBLK
                 134 LDLP:
7867 3655        135         MVI     M,55H
7869 23          136         INX     H
786A 3ECE        137         MVI     A,0CEH
786C BC          138         CMP     H
786D C26778      139         JNZ     LDLP
                 140 ;
                 141 ;
7870 3EFF        142         MVI     A,0FFH
7872 77          143         MOV     M,A               ;INSERT END OF DATA STRING
                 144                                   ;MARKER
                 145 ;
```

```
LOC  OBJ        LINE       SOURCE STATEMENT

                  146 ;
                  147 ;     INITIATE DATA TRANSFER
                  148 ;
                  149 ;
7873 210080       150         LXI     H,STRADD
7876 224478       151         SHLD    DESADD          ;STORE STARTING ADDRESS OF
                  152                                 ;E2 BOARD
7879 2100C0       153         LXI     H,RAMBLK
787C 224278       154         SHLD    SRCADD          ;STORE STARTING ADDRESS OF
                  155                                 ;SOURCE RAM BLOCK
787F 7E           156         MOV     A,M             ;FETCH FIRST BYTE FROM SOURCE
7880 2A4478       157         LHLD    DESADD          ;LOAD DESTINATION ADDRESS
                  158                                 ;(E2 BOARD)
                  159 ;
                  160 STXFER:
7883 77           161         MOV     M,A             ;WRITE FIRST BYTE TO E2
                  162                                 ;BOARD
7884 3E01         163         MVI     A,1
7886 323F78       164         STA     E2BUSY          ;SET FLAG INDICATING THAT A
                  165                                 ;DATA TRANSFER IS IN PROGRESS
                  166 ;
                  167 ;
                  168 ;
                  169 ;
                  170 ;       THIS TIGHT LOOP SIMULATES AN ACTUAL SYSTEM CPU
                  171 ;       DOING ITS MAIN PROCESSING
                  172 ;
                  173 ;
                  174 PROCES:
7889 3A3F78       175         LDA     E2BUSY
788C FE01         176         CPI     1
788E CA8978       177         JZ      PROCES
                  178 ;
                  179 ;
                  180 ;
                  181 ;     ONCE THE DATA TRANSFER IS COMPLETED THE OPERATOR
                  182 ;     IS INFORMED AND CONTROL IS RETURNED TO ISIS
                  183 ;
                  184 ;
                  185 ;
                  186 ;
                  187 FINISH:
7891 212778       188         LXI     H,FINMSG
7894 224078       189         SHLD    MSGADD
7897 CDE578       190         CALL    DISMSG
                  191 ;
                  192 ;
                  193 ;
                  194 RTISIS:
789A 0E09         195         MVI     C,EXIT
789C 113B78       196         LXI     D,EBLK
789F CD0000   E   197         CALL    ISIS
                  198 ;
                  199 ;
                  200 ;
```

```
LOC  OBJ        LINE       SOURCE STATEMENT

                201 ERROR:
78A2 211A78     202        LXI     H,ERRMSG
78A5 224078     203        SHLD    MSGADD
78A8 CDE578     204        CALL    DISMSG
78AB C39A78     205        JMP     RTISIS
                206 ;
                207 ;
                208 ;
                209 ;*****************************
                210 ;
                211 ;
                212 ;      SUBROUTINES
                213 ;
                214 ;
                215 ;
                216 ;
                217 ;
                218 ;      WHEN THE E2 BOARD HAS COMPLETED ITS BYTE
                219 ;      ERASE/WRITE CYCLE THIS ROUTINE WILL VERIFY
                220 ;      THE WRITTEN DATA.  THE NEXT BYTE IS FETCHED
                221 ;      FROM THE RAM BLOCK AND WRITTEN TO THE NEXT
                222 ;      LOCATION ON THE E2 BOARD.
                223 ;
                224 ;
                225 ;
                226 ;
                227 SRVINT:
78AE FB         228        EI
                229 ;
                230 ;      SAVE ALL REG'S
                231 ;
78AF F5         232        PUSH    PSW
78B0 C5         233        PUSH    B
78B1 D5         234        PUSH    D
78B2 E5         235        PUSH    H
78B3 D300       236        OUT     0               ;RESET THE E2 BOARD
                237 ;
78B5 2A4478     238        LHLD    DESADD
78B8 7E         239        MOV     A,M
78B9 2A4278     240        LHLD    SRCADD
78BC BE         241        CMP     M               ;CORRECT DATA?
78BD C2A278     242        JNZ     ERROR
                243 ;
                244 ;      YES, CONTINUE
                245 ;
78C0 23         246        INX     H
78C1 7E         247        MOV     A,M
78C2 FEFF       248        CPI     0FFH            ;END OF STRING MARKER?
78C4 CAD578     249        JZ      DONE
                250 ;
                251 ;      NO, CONTINUE
                252 ;
78C7 224278     253        SHLD    SRCADD
78CA 2A4478     254        LHLD    DESADD
78CD 23         255        INX     H
```

```
LOC  OBJ        LINE       SOURCE STATEMENT

78CE 77          256        MOV     M,A             ;WRITE NEW BYTE TO E2 BOARD
78CF 224478      257        SHLD    DESADD
78D2 C3DA78      258        JMP     REST            ;RESTORE REG'S AND RETURN
                 259 ;
                 260 ;    CLEAR FLAG TO INFORM CPU THAT THE DATA TRANSFER
                 261 ;    IS FINISHED
                 262 ;
                 263 DONE:
78D5 3E00        264        MVI     A,0
78D7 323F78      265        STA     E2BUSY
                 266 ;
                 267 REST:
78DA E1          268        POP     H
78DB D1          269        POP     D
78DC C1          270        POP     B
78DD F3          271        DI
78DE 3E20        272        MVI     A,20H
78E0 D3FD        273        OUT     OLRSTR
78E2 F1          274        POP     PSW
78E3 FB          275        EI
78E4 C9          276        RET
                 277 ;
                 278 ;
                 279 ;
                 280 ;
                 281 ;
                 282 ;
                 283 DISMSG:
78E5 2A4078      284        LHLD    MSGADD
                 285 MSGLP:
78E8 4E          286        MOV     C,M
78E9 3EFF        287        MVI     A,0FFH
78EB BE          288        CMP     M
78EC C8          289        RZ
78ED CD0000   E  290        CALL    CO
78F0 23          291        INX     H
78F1 C3E878      292        JMP     MSGLP
                 293 ;
                 294 ;
                 295 ;
                 296 ;    RAM BLOCK
C000             297        ORG     0C000H
C000             298 RAMBLK:        DS      1000H
                 299 ;
                 300 ;
                 301 ;
                 302 ;
7846             303        END     INIT


PUBLIC SYMBOLS


EXTERNAL SYMBOLS
CI     E 0000    CO     E 0000    ISIS   E 0000
```

```
USER SYMBOLS
CI     E 0000   CO     E 0000   CR     A 000D   DESADD A 7844   DISMSG A 78E5   DONE   A 78D5   E2BUSY A 783F
EBLK   A 783B   ERRMSG A 781A   ERROR  A 78A2   ESTAT  A 783D   EXIT   A 0009   FINISH A 7891   FINMSG A 7827
INIT   A 7846   INTMSK A 00FC   ISIS   E 0000   LDLP   A 7867   LF     A 000A   MAINPG A 7864   MSGADD A 7840
MSGLP  A 78E8   OLRSTR A 00FD   PROCES A 7889   RAMBLK A C000   REST   A 78DA   RTISIS A 789A   SRCADD A 7842
SRVINT A 78AE   STRADD A 8000   STXFER A 7883   TRNMSG A 7803

ASSEMBLY COMPLETE,  NO ERRORS
```

16-BIT DATA BUS STRUCTURE

The Multibus card can use either an 8-bit or 16-bit data bus. The PROM Array is organized in pairs of 8-bit wide MOS PROM's to enable the formation of a 16-bit word. For a 16-bit data bus, the upper byte MOS PROM is enabled whenever $\overline{\text{BHE}}$ (Byte High Enable) is low. The lower byte PROM is enabled when A0 is low. The upper and lower PROM's can be enabled and accessed separately as individual bytes or together to form a word. Accessing data by words takes half the time required to do byte operations; thus the advantage of 16-bit systems over 8-bit systems.

HARDWARE DESCRIPTION

Overview

This discussion assumes an 8-bit data bus is being used and applies equally to a 16-bit-wide system except that whenever a byte-wide operation is being described, two bytes (two MOS PROMs) in parallel are being affected.

The E^2 Board hardware consists of the following sections:

1. Sequencing and Timing
2. $\overline{\text{XACK}}$ Generation
3. Bus Address Decoding
4. PROM Array Decoding
5. Data and Address Latches and Buffers
6. V_{PP} and $\overline{\text{OE}}$ Drivers
7. 5V to 24V Converter
8. Write Protection Circuitry

See the block diagram in Figure 8.

A brief description of the function of each circuit block will be given. The circuit operation will then be discussed in detail in the subsections to follow.

The Sequencing and Timing circuitry generates the signals necessary to do the byte erase, byte write, chip erase cycles, and read cycles on the E^2 PROMs.

The $\overline{\text{XACK}}$ Generator returns the $\overline{\text{Transfer Acknowledge}}$ signal to the Multibus Bus Master after receiving any memory or I/O command.

The bus Address Decoder performs 2 functions:

1. Enabling the E^2 Board within its assigned address block for memory operations.
2. Enabling the RESET function and setting the Chip Erase Mode whenever the proper I/O addresses are written to.

The PROM Array Decoder enables the proper MOS PROM for any given memory address.

The Address and Data Latches hold the Bus address and data values for the duration of the E^2 write and Chip Erase operations. During read operations, the Data Buffers transfer the accessed data to the Multibus.

The V_{PP} and $\overline{\text{OE}}$ Drivers provide the high voltage pulses required for the byte erase, byte write, and Chip Erase cycles while the 5V to 24V Converters provide the supply voltage for the V_{PP} and $\overline{\text{OE}}$ drivers. Tied to these circuits is the Write Protection Circuitry which prevents any spurious write cycles from occurring during the system power up and power down transitions.

The figures referenced in the following subsections are shown in the Schematic Section.

Sequencing and Timing

READ OPERATION

When $\overline{\text{MRDC}}$ goes low the $\overline{\text{RDEN}}$ signal also goes low. $\overline{\text{WR Mode}}$ is normally high when the E^2 Board is not being accessed and is not performing an operation. $\overline{\text{WR Mode}}$ also stays high during a Read operation. The address latches in Figure 12 remain transparent, and lines BAC–BAF select one of the MOS PROMs in the PROM Array via the 3628A Bipolar PROM decoder. In Figure 13 the $\overline{\text{RDEN}}$ signal enables the 8287 transceivers to gate the output data onto the multibus. $\overline{\text{RDEN}}$ also causes $\overline{\text{OE}}$ to go low to read the data out of the MOS PROMs.

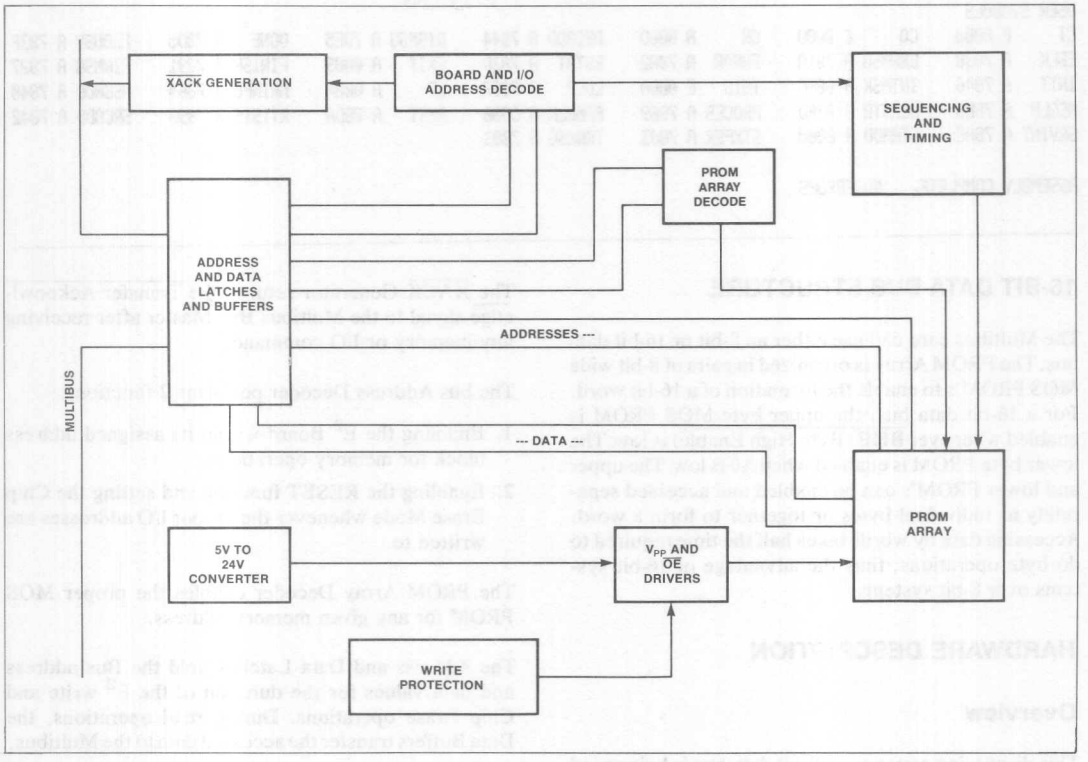


Figure 8. E^2 Board Block Diagram

WRITE OPERATION

Refer to Figures 10 and 11 and to the timing diagram in Figure 9.

When $\overline{MWTC}$ goes low the $\overline{BD\ WR}$ signal also goes low which sets the $\overline{WR}$ Mode FF. The falling edge of $\overline{WR\ Mode}$ latches the addresses as the falling edge of $\overline{BD\ WR}$ latches the data. The rising edge of BD WR sets the Start Erase Cycle FF, which in turn starts the one-shot chain.

The first one-shot delays the rising edge of V_{PP} to provide some set-up time for $\overline{CE}$. When the delay one-shot times out, it triggers the V_{PP} ON one-shot. This second one-shot turns on the V_{PP} driver for approximately 10ms. This is the byte erase cycle. Although the bus data has been latched, the latch outputs are not yet enabled by $\overline{Data\ In\ En}$ (Figure 13). The 1K pullup resistors on the LD0–LD15 lines pull the high-impedance latch outputs up to 5V. As a result, the data inputs to the E^2PROM are all 1's which in turn erase the addressed data byte. When the V_{PP} ON one-shot times out, the V_{PP} Discharge one-shot is triggered. The V_{PP} driver is now shut off ($\overline{V_{PP}\ ON}$ = 1) but the voltage on the V_{PP} line will take a long time to discharge to 5V. This is due to the 4.7 uf low-frequency decoupling capacitor, connected from V_{PP} to ground; the capacitor is needed to suppress low frequency noise (See Figure 17). In order to pull the V_{PP} line down fast, the V_{PP} Discharge signal turns on Q8 which discharges the capacitor. When the third one-shot times out, the Cycle Done One-Shot starts, which clears the start Erase Cycle FF and forces $\overline{CE}$ high (Figure 16 and Figure 10). The rising edge of Cycle Done sets the Start Write Cycle FF and causes the 74LS393 counter (Figure 10) to increment from 0 to 1. This starts the one-shot chain again to perform the byte write cycle. The $\overline{Data\ In\ En}$ signal enables the latched data onto the input lines. The one-shot chain then delays, activates V_{PP}, and discharges the V_{PP} line. This time the data byte is written into the selected 2816 address location. The 74LS393 counter is incremented a second time and its QB output lowers one of the Multibus Interrupt Lines. The CPU RESETS the E^2 board with an $\overline{IOWC}$ command. The WR Mode FF, the Start Write FF and the 74LS393 counter are cleared, and the E^2 Board is ready for the next operation.

CHIP ERASE OPERATION

The Chip Erase Operation is quite similar to the byte erase operation. The differences are:

1. The Chip Erase FF is set by the Multibus CPU before initiating the write operation. The Chip Erase FF is set by doing an $\overline{\text{IOWC}}$ command to the Chip Erase address.
2. When the write operation begins, the $\overline{\text{OE}}$ signal is raised to 14.5V (Figure 17). The byte erase cycle proceeds as before.
3. At the end of the byte erase cycle the Cycle Done signal does not set the Start Write Cycle FF. Instead, the Start Write Cycle FF is held in a clear state by the $\overline{\text{INH}}$ Byte Write signal shown in Figure 10. Cycle Done increments the 74LS393 counter from 0 to 1. The Q_A output is now used to lower one of the Interrupt Lines to signal the CPU that the Chip Erase Operation is complete. When the CPU resets the E^2 Board, the Chip Erase FF is also cleared.

INITIALIZATION

The E^2 Board must be RESET after power up. Due to the write protection circuitry delay period after power up, the RESET should not be sent until at least 1 second after the CPU starts running. Once the board is RESET, it is ready for a command.

$\overline{\text{XACK}}$ Generation

(Figure 11) The $\overline{\text{XACK}}$ ($\overline{\text{Transfer}}$ $\overline{\text{Acknowledge}}$) signal is driven low after a delay period determined by the t_{ACC} of the slowest MOS PROM in the PROM Array. $\overline{\text{XACK}}$ stays low until the Memory or I/O command goes back high. See the XACK delay subsection.

Bus Address Decoding

Two sets of addresses need to be decoded for the E^2 Memory Board: the memory space address for the PROM Array and the I/O address for Chip Erase Mode and the RESET function. The 74LS85 comparators in Figure 16, along with Jumpers J9–J12 and J13–J19, are used to select the desired addresses and generate the appropriate enabling signals when the selected addresses appear on the Multibus. The board memory address is determined by jumpers J9–J12. When the correct memory address is put on the bus, the $\overline{\text{MEM}}$ $\overline{\text{EN}}$ signal goes low. The $\overline{\text{INH1}}$ ($\overline{\text{INHIBIT}}$ $\overline{\text{RAM}}$) signal is driven low on the Multibus to disable any RAM memory that is occupying the same memory space as the E^2 Board.

When the selected I/O address appears on the system bus and $\overline{\text{IOWC}}$ goes low the $\overline{\text{BD}}$ $\overline{\text{IOW}}$ signal goes low (Figure 16). If ADR0 is low, the RESET function is activated. If ADR0 is high, the Chip Erase FF is set.

MOS PROM Array Decoder

(Figure 12) Details on how to program the 3628A Bipolar PROM decoder are given in the Installation Instructions under PROM Array Decoder. The 3628A acts as a sophisticated decoder. The address input to the 3628A allows a maximum address range of 64K with a minimum resolution of 2K. The A0 and BHEN input signals enable the 3628A to select the lower byte MOS PROM, the upper byte MOS PROM, or both in parallel. The 3628A output lines connect to an 8282 8-bit latch. The 8282 latches the decoder output to provide $\overline{\text{CE}}$ for the 10ms erase and write cycles. During read cycles the 8282 simply acts as a buffer for the decoder.

Address and Data Latches and Buffers

The 8283s and 8282 of Figures 12 and 13 latch the address and data from the Multibus when the CPU issues an $\overline{\text{MWTC}}$ command. These address and data values stay latched throughout the Write Operation. The addresses are latched on the falling edge of $\overline{\text{WR}}$ Mode. The input data from the bus is latched by the falling edge of $\overline{\text{WR}}$ EN (See Figure 13). For Read operations the $\overline{\text{WR}}$ Mode signal stays high. A high on the 8283 STB input puts these latches in "transparent" mode: they act as buffers for the bus addresses. The 8287s in Figure 13 act as data output buffers for the accessed MOS PROM data.

The 8286 is used when the system data bus is 8-bits wide. This transceiver transfers the data byte from the LD0–LD7 low byte data bus to LD8–LD15 upper byte data bus for write operations. For read operations, the data byte from the LD8–LD15 byte bus is transferred to the LD0–LD7 data byte bus. This byte swapping circuit is actually adapting the 16-bit upper/lower byte structure to an external 8-bit wide data bus. See the section on 16-bit Data Bus Structure for more information.

V_{PP} and $\overline{\text{OE}}$ Drivers

Refer to Figure 17. The V_{PP} driver provides the 21V V_{PP} programming pulse for the 2816. The pulse goes from 5V to 21V with an exponential rising edge. The $\overline{\text{OE}}$ driver is used to provide nominal TTL levels for read and write operations. This driver also provides a 14.5V level for the Chip Erase cycle.

5V to 24V Converter

Refer to Applications Note AP-103 in the E^2PROM Applications Handbook. (Also Figure 18.)

Write Protection Circuitry

The Write Protection circuits are designed to prevent the TTL control logic from causing an E^2 write/erase cycle to occur during the periods of board power up or power down. The 747 op-amp in Figure 18 senses when the board 5V supply has dropped below the voltage level on C41. When this happens, the op-amp disables the V_{PP} driver by grounding C38 (Figure 17). This prevents the capacitor from charging up the 21V—it is the exponential rising voltage on this capacitor which is used to generate the V_{PP} programming pulse's rising edge.

When the E^2 Board is powered up, the rising V_{CC} voltage begins charging up capacitor C30. Until the voltage on C30 is high enough to turn on Q4 (approximately 3.5V), this transistor will hold the $\overline{V_{PP}\ OFF}$ signal low. This is the same signal in Figures 18 and 17 that is used by the power-down circuit described above. This keeps the V_{PP} driver disabled until about 500ms after V_{CC} reaches 5V. About 400ms before V_{CC} reaches 5V, the Write Protect FF in Figure 10 is set by the Multibus $\overline{INIT}$ signal. This FF will hold the V_{PP} ON one-shot disabled until the CPU RESETS the E^2 Memory Board and the Write Protect FF. Thus, the Q4/C30 circuit holds the V_{PP} driver off until long after the TTL logic has stabilized and the Write Protect FF has disabled the V_{PP} ON one-shot.

The purpose of the Write Protect Flip Flop is to prevent the 2816s from being written to by the Intellec Monitor Program immediately after power up. The Intellec Monitor tries to write to every location in its addressable range after power up. This is done to determine how much RAM is in the system. In a non-Intellec system the $\overline{INIT}$ signal is not really needed as long as no System Write commands occur other than those generated by the user.

SCHEMATIC DIAGRAMS

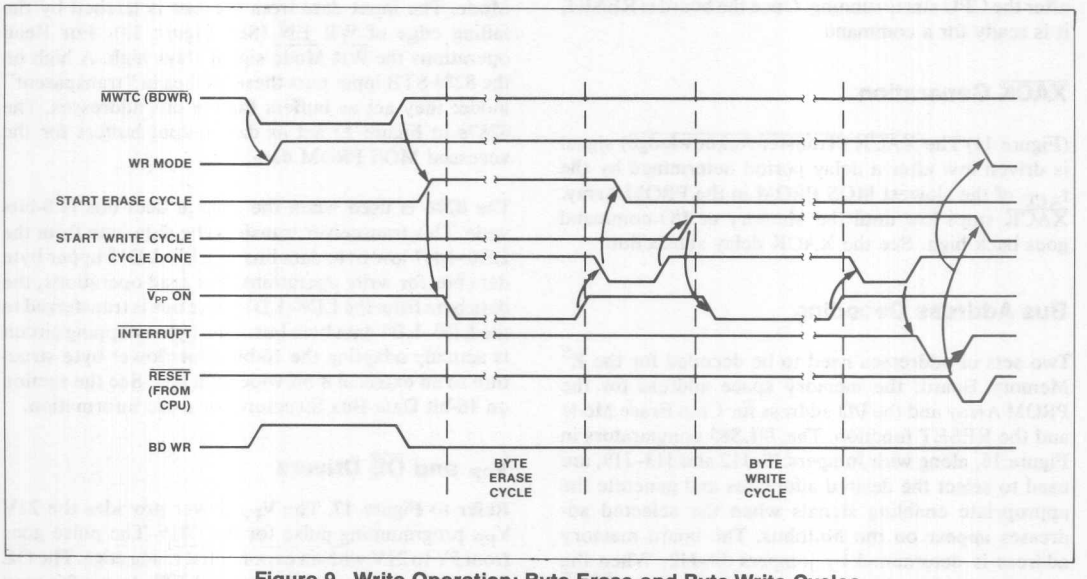


Figure 9. Write Operation: Byte Erase and Byte Write Cycles

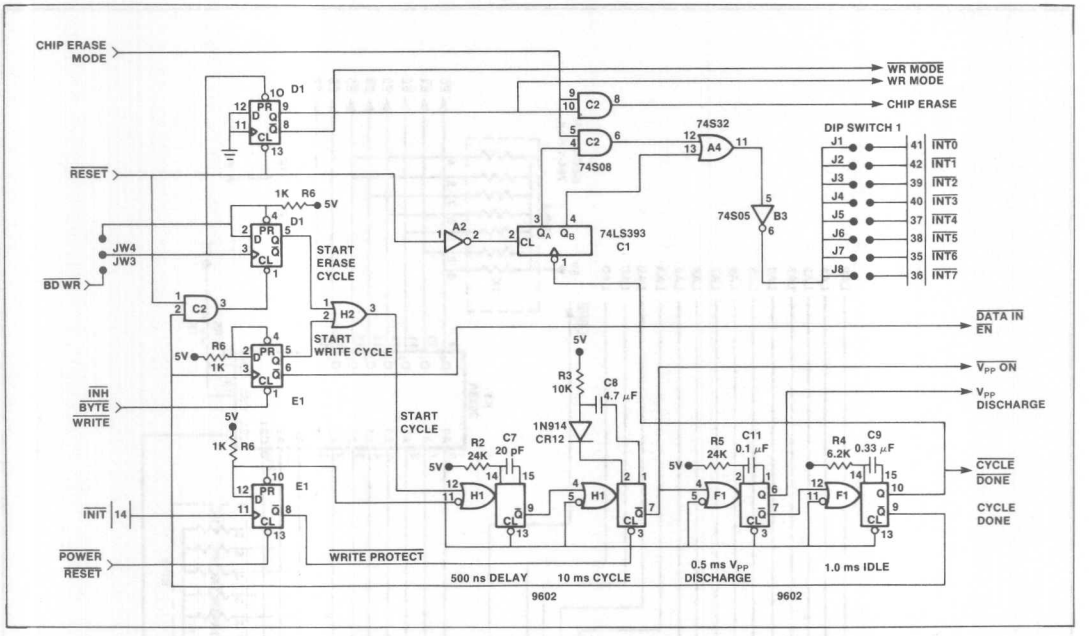
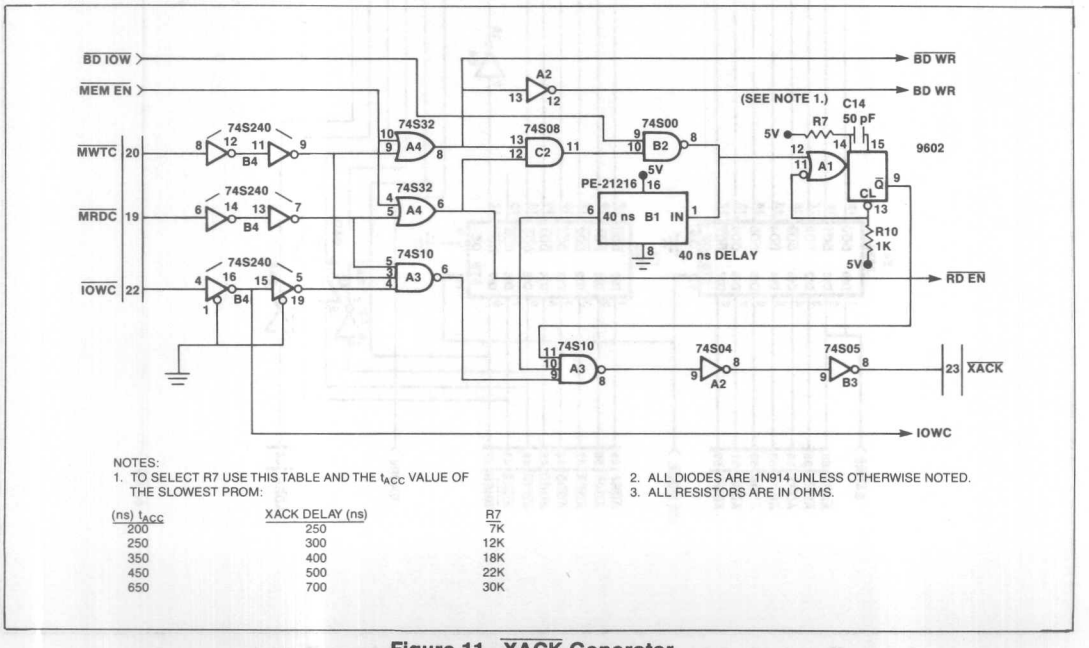


Figure 10. Write and Erase Sequencing and Timing



NOTES:
1. TO SELECT R7 USE THIS TABLE AND THE t_{ACC} VALUE OF THE SLOWEST PROM:

(ns) t_{ACC}	XACK DELAY (ns)	R7
200	250	7K
250	300	12K
350	400	18K
450	500	22K
650	700	30K

2. ALL DIODES ARE 1N914 UNLESS OTHERWISE NOTED.
3. ALL RESISTORS ARE IN OHMS.

Figure 11. $\overline{\text{XACK}}$ Generator

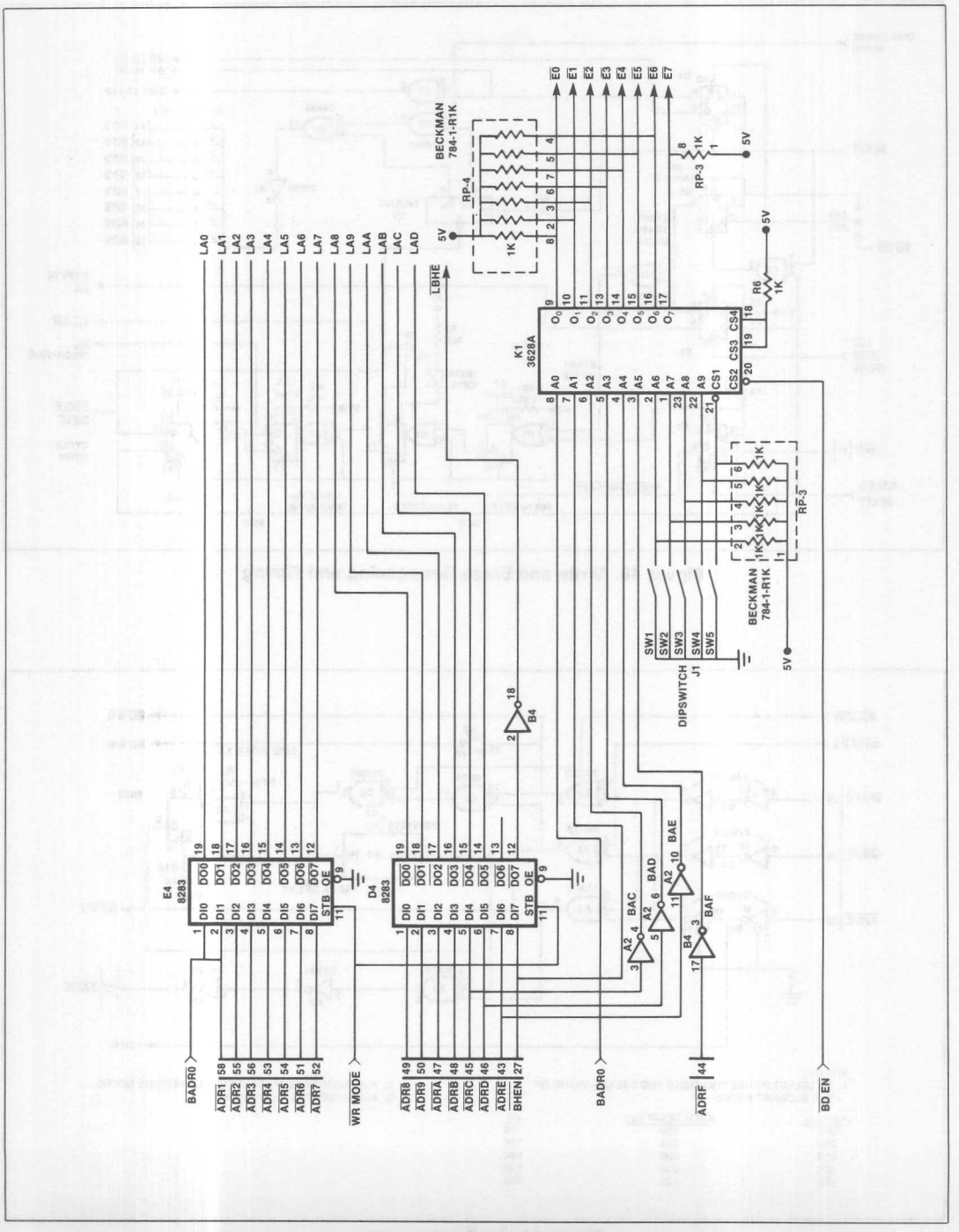


Figure 12. Address Latches and MOS PROM Array Decoder

AFN-02067A

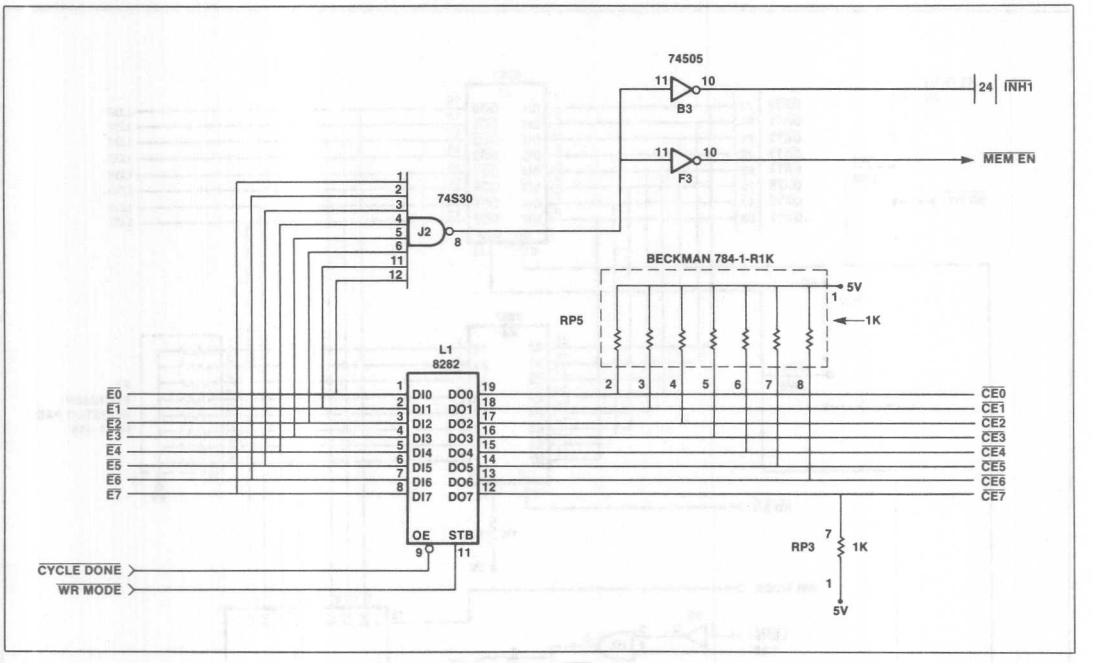


Figure 12a. $\overline{CE}$ Latch

AFN-02067A

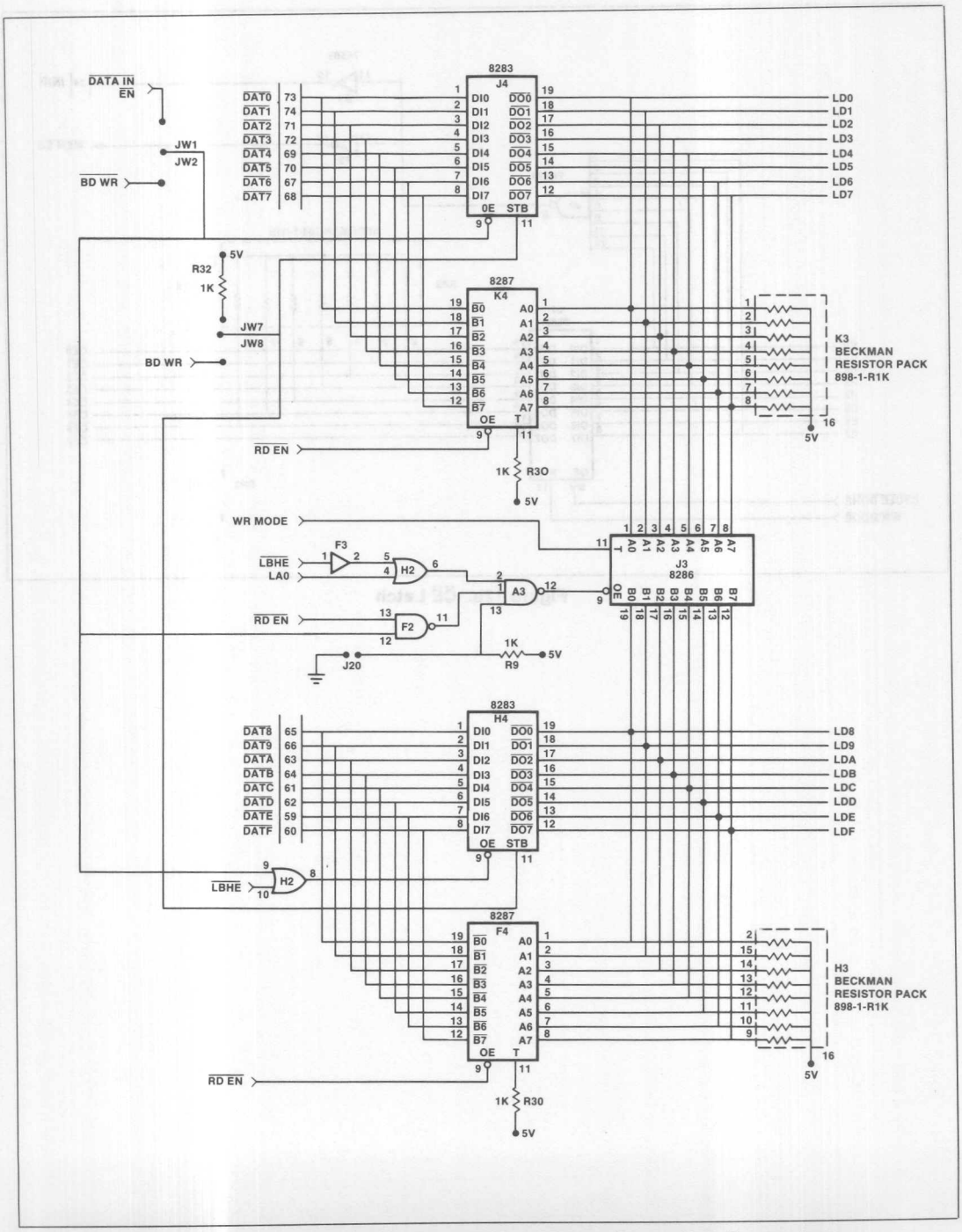


Figure 13. Data In Latch, Data Out Buffer, and Upper/Lower Byte Transceiver

AFN-02067A

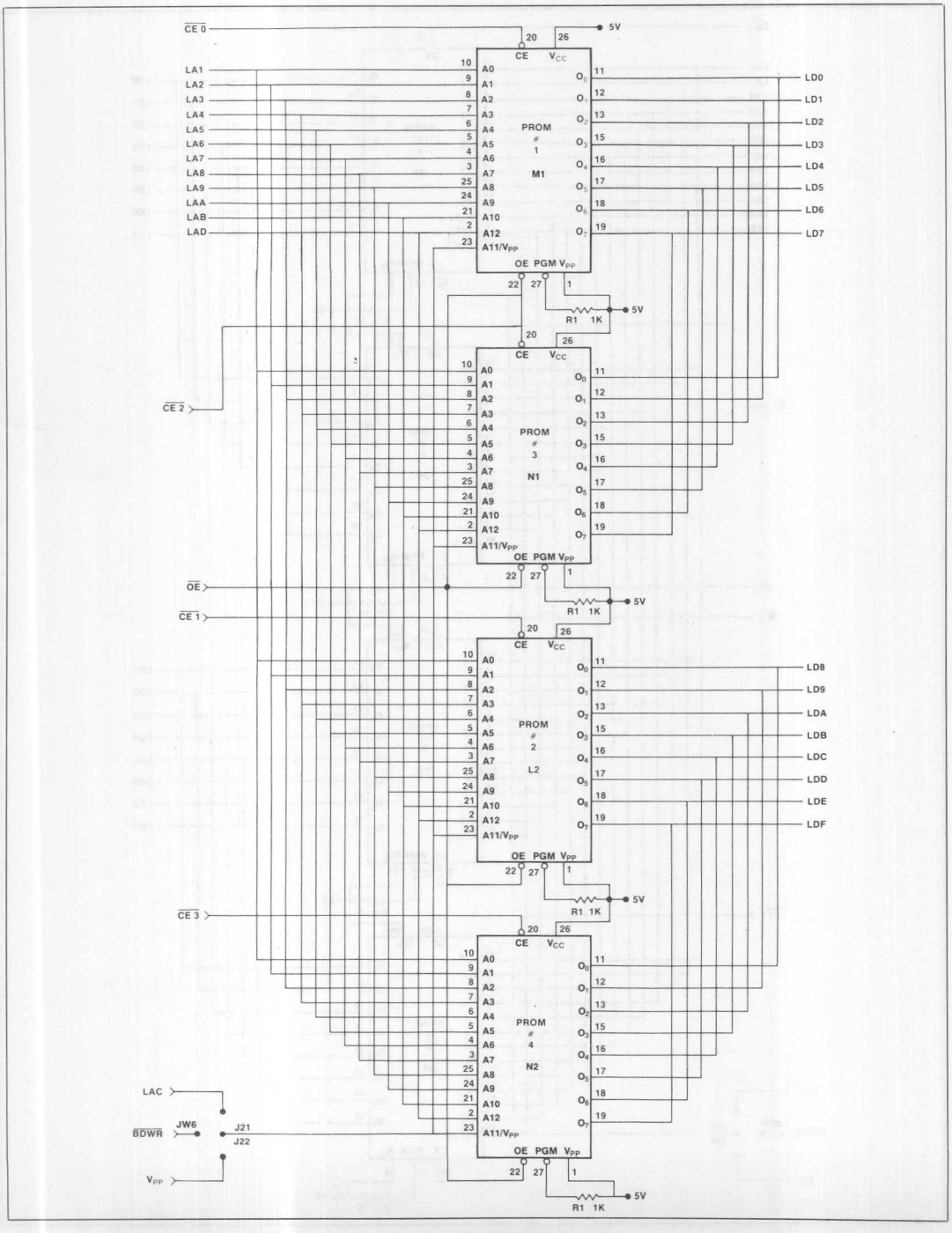


Figure 14. MOS PROM Array

AFN-02067A

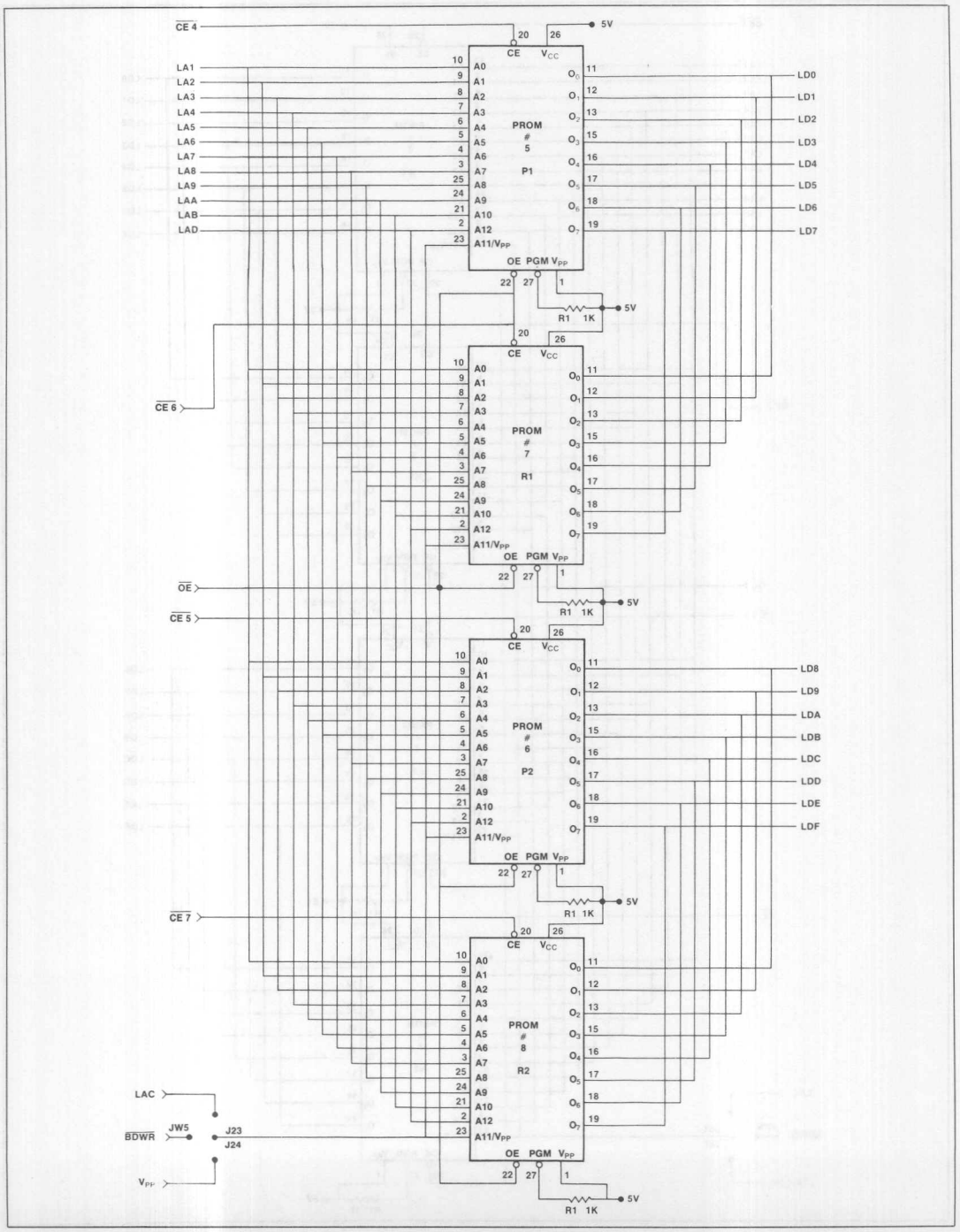


Figure 15. MOS PROM Array

AFN-02067A

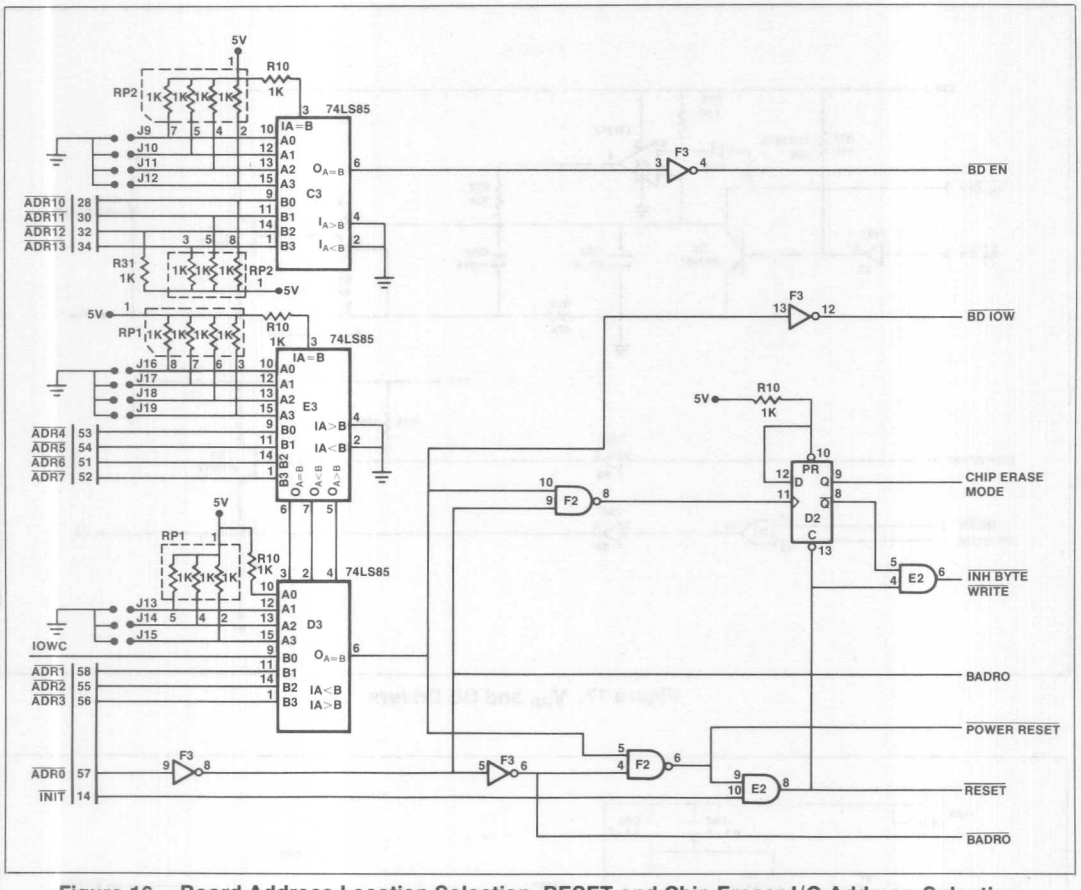


Figure 16. Board Address Location Selection, RESET and Chip Eraser I/O Address Selection

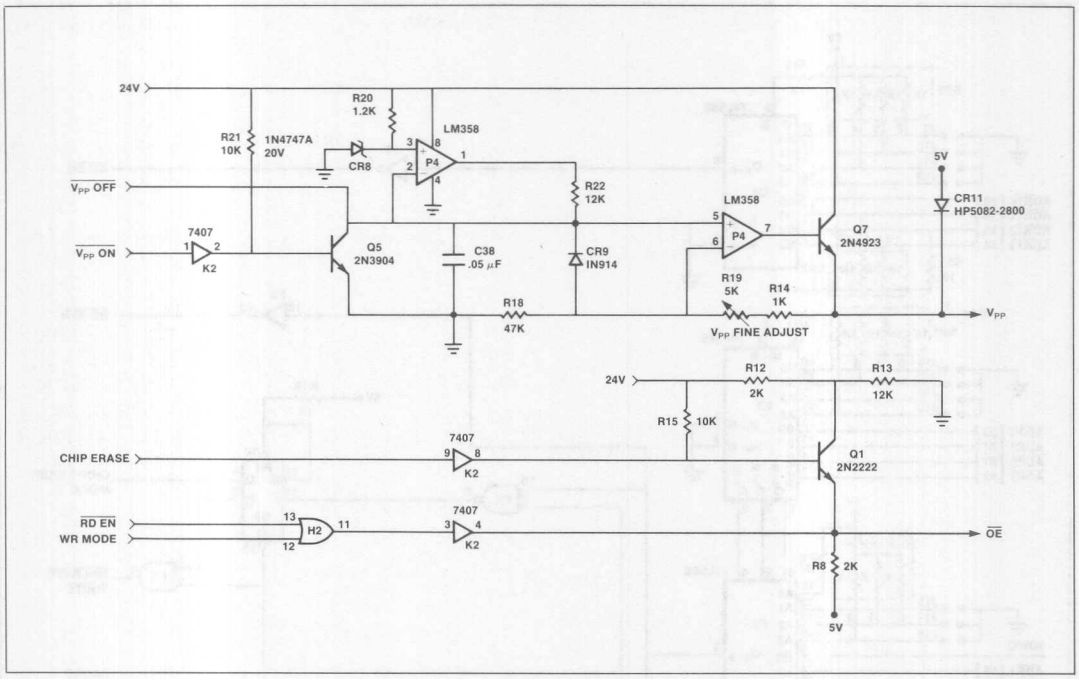


Figure 17. V_{PP} and OE Drivers

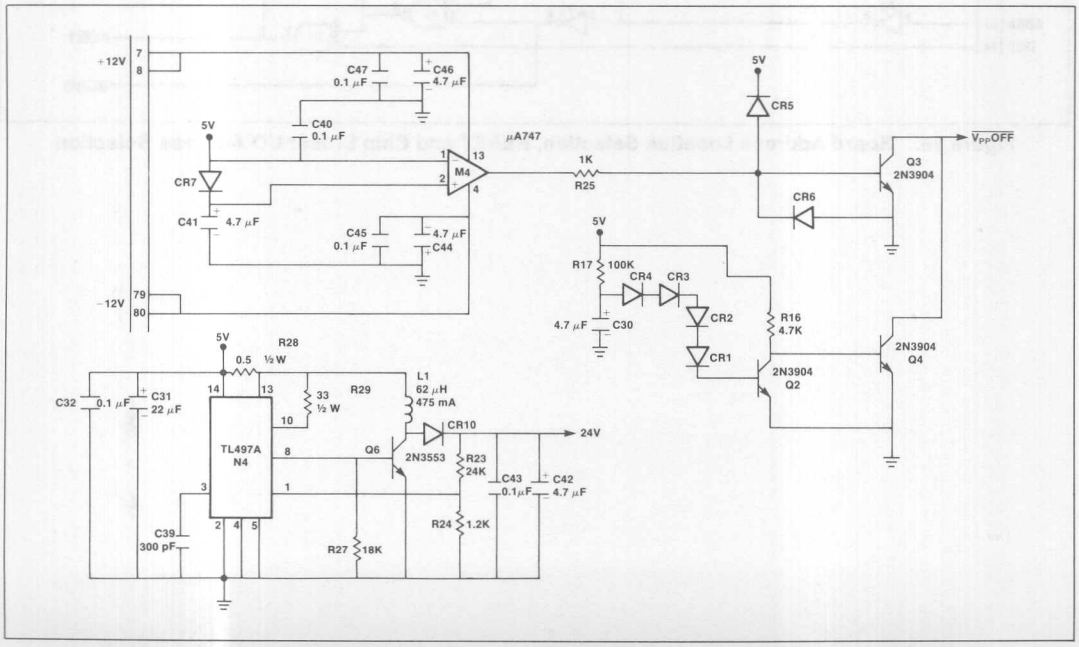


Figure 18. 5V to 23V Converter and Power Up/Power Down Write Protection Circuitry

ASSEMBLY INSTRUCTIONS

1. Install and solder the following Integrated Circuits:

A4	— 74S32	A2	— 74S04
B4	— 74S240	B2	— 74S00
D4	— 8283	C2	— 74S08
E4	— 8283	D2	— 74LS74
F4	— 8287	E2	— 74LS08
H4	— 8283	F2	— 74LS00
J4	— 8283	H2	— 74LS32
K4	— 8287	J2	— 74S30
A3	— 74S10	K2	— 7407
B3	— 74S05	A1	— 9602
C3	— 74LS85	B1	— PE-21216
D3	— 74LS85	C1	— 74LS393
E3	— 74LS85	D1	— 74LS74
F3	— 74LS04	E1	— 74LS74
J3	— 8286	F1	— 9602
		H1	— 9602
		L1	— 8282
		N4	— TL497A
		M4	— UA747
		P4	— LM358

2. Install and solder a 24-pin socket at K1.

3. Install and solder 28-pin sockets at M1, L2, N1, N2, P1, P2, R1 and R2.

4. Install and solder jumper pin pairs at the following locations:

J1	J5	J13	J16
J2	J6	J14	J17
J3	J7	J15	J18
J4	J8		J19
J9		J20	
J10			
J11			
J12			

5. Break in half 4 jumper pairs.

   Install and solder one jumper pair at J21. Install and solder one of the single jumper pins at J22.

   Install and solder another single jumper pin and one jumper pair at J23 and J24.

   Install and solder jumper pairs at JW7, JW3, and JW2.

   Install and solder single jumper pins at JW8, JW4, JW1, JW6, and JW5.

6. Install and solder the Dipswitch at location J1.

7. Install and solder resistors and resistor networks at the following locations:

H3	— 898-1-R1K	R16	— 4.7K
K3	— 898-1-R1K	R17	— 100K
RP1	— 784-1-R1K	R29	— 33, 1/2 W
RP2	— 784-1-R1K	R28	— 0.5, 1/2 W
RP3	— 784-1-R1K	R27	— 18K
RP4	— 784-1-R1K	R24	— 1.2K
RP5	— 784-1-R1K	R23	— 24K
R6	— 1K	R15	— 10K
R5	— 24K	R22	— 12K
R4	— 6.2K	R21	— 10K
R3	— 10K	R20	— 1.2K
R2	— 24K	R18	— 47K
R1	— 1K	R12	— 2K
R32	— 1K	R13	— 12K
R10	— 1K	R14	— 1K
R9	— 1K	R25	— 1K
R8	— 2K		
R19	— 5K Mini-potentiometer		
R31	— 1K		
R30	— 1K		

8. Install and solder capacitors in the following locations:

C13	— 0.1 μf	C19	— 0.1 μf
C12	— 0.1 μf	C18	— 0.1 μf
C11	— 0.1 μf	C17	— 0.1 μf
C10	— 0.1 μf	C16	— 0.1 μf
C9	— 0.33 μf	C15	— 0.1 μf
C8	— 4.7 μf	C28	— 0.1 μf
C7	— 20 pf	C27	— 0.1 μf
C6	— 0.1 μf	C26	— 0.1 μf
C5	— 0.1 μf	C25	— 0.1 μf
C4	— 0.1 μf	C24	— 0.1 μf
C3	— 0.1 μf	C37	— 0.1 μf
C2	— 0.1 μf	C49	— 22 μf
C1	— 0.1 μf	C36	— 0.1 μf
C23	— 0.1 μf	C35	— 0.1 μf
C22	— 0.1 μf	C34	— 0.1 μf
C21	— 0.1 μf	C33	— 0.1 μf
C20	— 0.1 μf	C48	— 22 μf

9. Install and solder the following diodes:

CR1	— 1N914	CR7	— 1N914
CR2	— 1N914	CR8	— 1N4747A
CR3	— 1N914	CR9	— 1N914
CR4	— 1N914	CR10	— 1N914
CR5	— 1N914	CR11	— HP5082-2800
CR6	— 1N914	CR12	— 1N914

10. Install and solder the following transistors:

Q1	—	2N2222A
Q2	—	2N3904
Q3	—	2N3904
Q4	—	2N3904
Q5	—	2N3904
Q6	—	2N3553

If hardware is provided or available, mount transistors in the following locations:

Q7	—	2N4923

Solder the leads of Q7 and Q8 to the solder pads on the board.

11. Install and solder the following capacitors:

C40	—	0.1 μf	C41	—	4.7 μf
C47	—	0.1 μf	C44	—	4.7 μf
C45	—	0.1 μf	C42	—	4.7 μf
C39	—	300 pf	C31	—	22 μf
C43	—	0.1 μf	C30	—	4.7 μf
C38	—	0.05 μf	C46	—	4.7 μf
C32	—	0.1 μf			

12. Install and solder the 62 μh RF choke at location L1 (just above the 60-pin edge connector).

APPENDIX A
JUMPER LIST

J1 $\overline{\text{INT0}}$
J2 $\overline{\text{INT1}}$
J3 $\overline{\text{INT2}}$
J4 $\overline{\text{INT3}}$
J5 $\overline{\text{INT4}}$
J6 $\overline{\text{INT5}}$
J7 $\overline{\text{INT6}}$
J8 $\overline{\text{INT7}}$

J9 (ADR10)
J10 (ADR11)
J11 (ADR12)
J12 (ADR13)

4 bit selection of one of 16 64K pages for board address
—Note: these ADRs are in HEX

J13 (ADR1)
J14 (ADR2)
J15 (ADR3)
J16 (ADR4)
J17 (ADR5)
J18 (ADR6)
J19 (ADR7)

Select I/O address for Chip Erase Mode (ADR 0=1) and RESET function (ADR 0=0)

J20 Jumpered for 16-bit wide data bus, Open for 8-bit wide data bus.

NOTE: The proper decoding algorithm for the data bus must be used in the BIPOLAR PROM decoder—refer to the PROM Array Address Configuration subsection of the Installation Instructions.

J21 (Select 4K/8K)
J22 (Select 2K)

MOS PROMs 1–4

J23 (Select 4K/8K)
J24 (Select 2K)

MOS PROMs 5–8

JW1
JW2
JW3
JW4
JW5
JW6
JW7
JW8

8-bit wide static RAM

APPENDIX B
BIP DECODER DATA FORMAT
3628A, 1K X 8, 000-3FFH

Data = all 1's at all locations not shown.
0 = Switch is on
1 = Switch is off

SW4	SW3	SW2	SW1	(Hex) Address	(Hex) Data	Decoding for
0	0	0	0	2	FE	2K X 8
				3	FD	
				6	FB	(2816, 2815 OR 2716)
				7	F7	
				A	EF	
				B	DF	
				E	BF	
				F	7F	8-BIT DATA BUS
0	0	0	1	42	FE	
				43	FD	4K X 8
				46	FE	
				47	FD	(2732, 2732A)
				4A	FB	
				4B	F7	
				4E	FB	
				4F	F7	8-BIT DATA BUS
				52	EF	
				53	DF	
				56	EF	
				57	DF	
				5A	BF	
				5B	7F	
				5E	BF	
				5F	7F	
0	0	1	0	82	FE	
				83	FD	
				86	FE	
				87	FD	8K X 8
				8A	FE	
				8B	FD	(2764)
				8E	FE	
				8F	FD	
				92	FB	
				93	F7	8-BIT DATA BUS
				96	FB	
				97	F7	
				9A	FB	
				9B	F7	
				9E	FB	
				9F	F7	
				A2	EF	
				A3	DF	
				A6	EF	
				A7	DF	
				AA	EF	
				AB	DF	
				AE	EF	
				AF	DF	
				B2	BF	
				B3	7F	

SW4	SW3	SW2	SW1	(Hex) Address	(Hex) Data	Decoding for
0	0	1	0	B6	BF	8K × 8
				B7	7F	8-BIT DATA BUS
				BA	BF	(Continued)
				BB	7F	
				BE	BF	
				BF	7F	
0	0	1	1	C0	FC	2K X 8
				C1	FD	16-BIT DATA BUS
				C2	FE	
				C4	F3	(2816, 2815, OR 2716)
				C5	F7	
				C6	FB	
				C8	CF	
				C9	DF	
				CA	EF	
				CC	3F	
				CD	7F	
				CE	BF	
0	1	0	0	100	FC	4K X 8
				101	FD	16-BIT DATA BUS
				102	FE	
				104	FC	(2732 OR 2732A)
				105	FD	
				106	FE	
				108	F3	
				109	F7	
				10A	FB	
				10C	F3	
				10D	F7	
				10E	FB	
				110	CF	
				111	DF	
				112	EF	
				114	CE	
				115	DF	
				116	EF	
				118	3F	
				119	7F	
				11A	BF	
				11C	3F	
				11D	7F	
				11E	BF	
0	1	0	1	140	FC	8K X 8
				141	FD	16-BIT DATA BUS
				142	FE	
				144	FC	
				145	FD	
				146	FE	
				148	FC	(2764)
				149	FD	
				14A	FE	
				14C	FC	
				14D	FD	
				14E	FE	
				150	F3	
				151	F7	
				152	FB	
				154	F3	
				155	F7	
				156	FB	

SW4	SW3	SW2	SW1	(Hex) Address	(Hex) Data	Decoding for
0	1	0	1	158	F3	8K × 8
				159	F7	16-BIT DATA BUS
				15A	FB	(Continued)
				15C	F3	
				15D	F7	
				15E	FB	
				160	CF	
				161	DF	
				162	EF	
				164	CF	
				165	DF	
				166	EF	
				168	CF	
				169	DF	
				16A	EF	
				16C	CF	
				16D	DF	
				16E	EF	
				170	3F	
				171	7F	
				172	BF	
				174	3F	
				175	7F	
				176	BF	
				178	3F	
				179	7F	
				17A	BF	
				17C	3F	
				17D	7F	
				17E	BF	
0	1	1	0	1A2	FE	LOCATED AT 8000H
				1A3	FD	8-BIT DATA BUS
				1A6	FB	
				1A7	F7	(2716, 2816 OR 2815)
				1AA	EF	
				1AB	DF	
				1AE	BF	
				1A7	7F	
0	1	1	1	1E0	FC	LOCATED AT 8000H
				1E1	FD	16-BIT DATA BUS
				1E2	FE	
				1E4	F3	(2716, 2816 OR 2815)
				1E5	F7	
				1E6	FB	
				1E8	CF	
				1E9	DF	
				1EA	EF	
				1EC	3F	
				1ED	7F	
				1EE	BF	

APPENDIX C
PARTS LIST

Table C-1. Integrated Circuits

Qty	Description
1	3628A-4
4	8283
1	8286
2	8287
3	74LS85
1	74LS393
3	9602
3	74LS74
1	74LS08
1	74S10
1	74S30
1	74LS32
1	74LS04
1	74LS00
1	74S00
1	74S05
1	8282
1	74S08
1	74S04
1	74S32
1	74S240
1	LM358
1	TTL Delay Line PE-21216
1	μA747
1	7407
1	TL497A
36	TOTAL

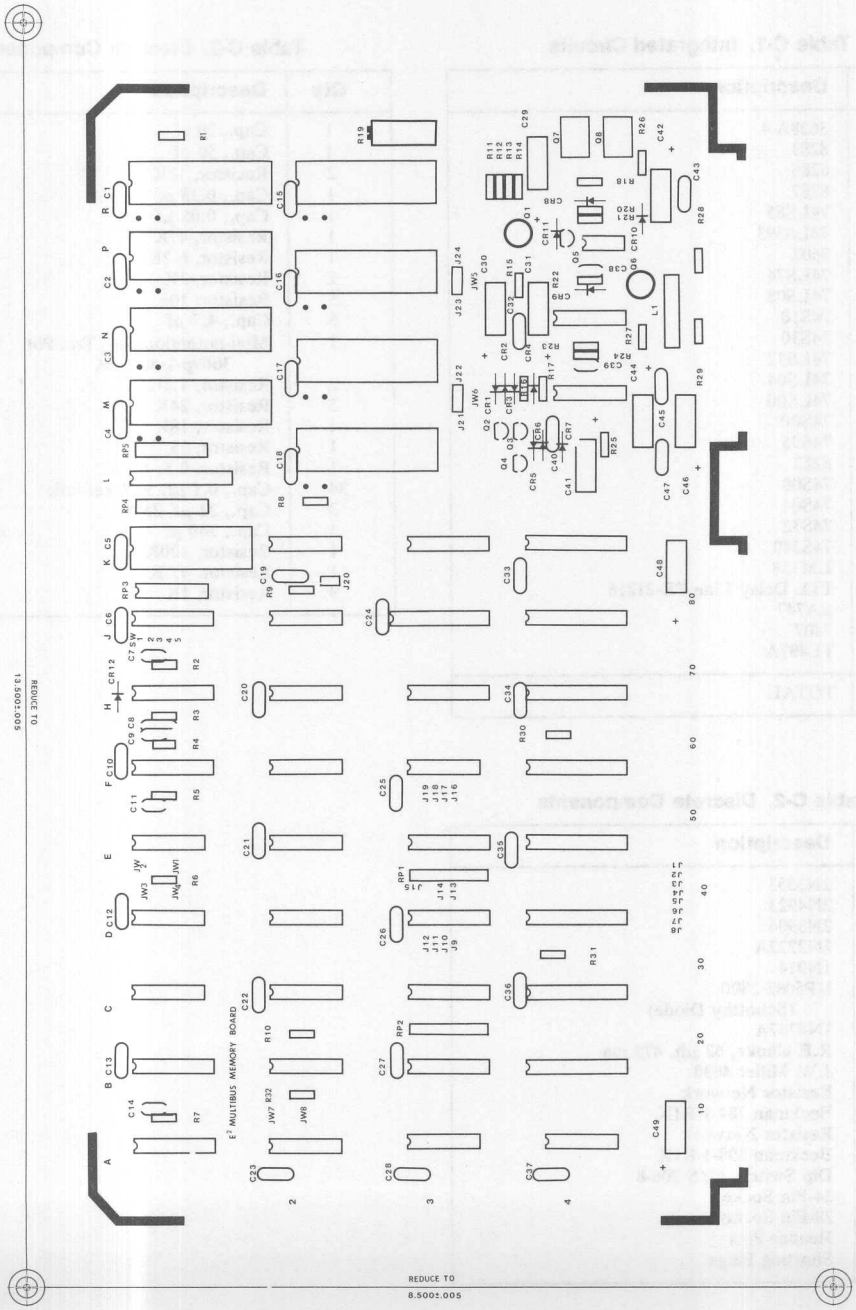
Table C-2. Discrete Components

Qty	Description
1	2N3553
1	2N4923
4	2N3904
1	2N2222A
11	1N914
1	HP5082-2800 (Schottky Diode)
1	1N4747A
1	R.F. Choke, 62 μh, 475 ma J.W. Miller 4630
5	Resistor Network Beckman 784-1-R1K
2	Resistor Network Beckman 898-1-R1K
1	Dip Switch, CTS 206-8
1	24-Pin Socket
8	28-Pin Sockets
29	Header Pins
18	Shorting Plugs

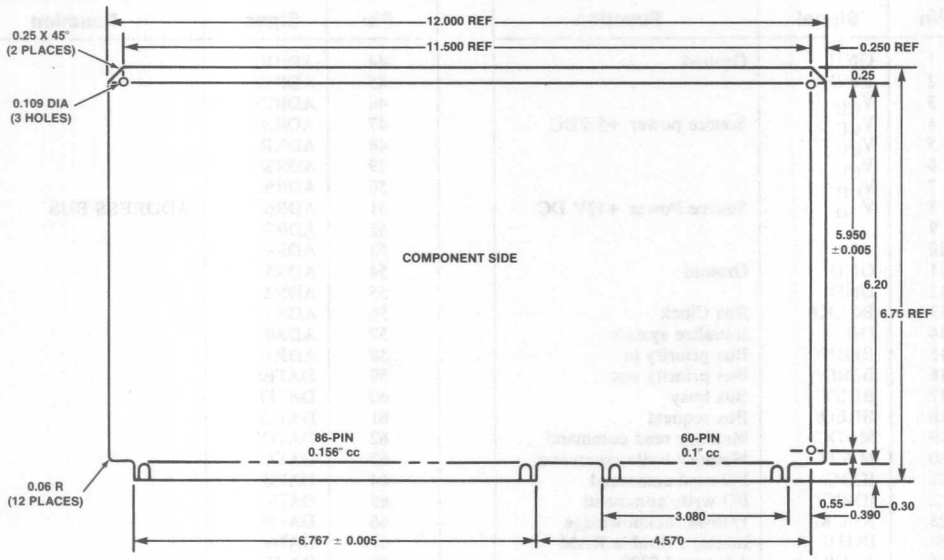
Table C-3. Discrete Components

Qty	Description
1	Cap., 20 pf
1	Cap., 50 pf
2	Resistor, 12K
1	Cap., 0.33 μf
1	Cap., 0.05 μf
1	Resistor, 47K
1	Resistor, 6.2K
2	Resistor, 2K
3	Resistor, 10K
6	Cap., 4.7 μf
1	Mini-potentiometer, TrimPot 3009p-1-502, 5K
2	Resistor, 1.2K
3	Resistor, 24K
1	Resistor, 18K
1	Resistor, 33, 1/2W
1	Resistor, 0.5, 1/2W
34	Cap., 0.1 μf, 50V, ceramic
3	Cap., 22 μf, 25V
1	Cap., 300 pf
1	Resistor, 100K
1	Resistor, 4.7K
9	Resistor, 1K

APPENDIX D
ASSEMBLY DRAWING



APPENDIX E
MULTIBUS PCB DIMENSIONS



AFN-02067A

APPENDIX F
MULTIBUS SIGNAL LIST

Pin	Signal	Function
1	GND	Ground
2	GND	
3	V_{CC}	
4	V_{CC}	Source power +5 VDC
5	V_{CC}	
6	V_{CC}	
7	V_{DD}	
8	V_{DD}	Source Power +12V DC
9		
10		
11	GND	Ground
12	GND	
13	BCLK/	Bus Clock
14	INIT/	Initialize system
15	BPRN/	Bus priority in
16	BPRO/	Bus priority out
17	BUSY/	Bus busy
18	BREQ/	Bus request
19	MRDC/	Memory read command
20	MWTC/	Memory write command
21	IORC/	I/O read command
22	IOWC/	I/O write command
23	XACK/	Transfer acknowledge
24	INH1/	Inhibit 1 disable RAM
25	AACK/	Advanced 8080 acknowledge
26		
27	BHEN/	Byte High Enable
28	AD10/	
29		
30	AD11/	
31		
32	AD12/	
33		
34	AD13/	
35	INT6/	
36	INT7/	
37	INT4/	External Interrupt
38	INT5/	Level Requests
39	INT2/	
40	INT3/	
41	INT0/	
42	INT1/	
43	ADRE/	ADDRESS BUS

Pin	Signal	Function
44	ADRF/	
45	ADRC/	
46	ADRD/	
47	ADRA/	
48	ADRB/	
49	ADR8/	
50	ADR9/	
51	ADR6/	ADDRESS BUS
52	ADR7/	
53	ADR4/	
54	ADR5/	
55	ADR2/	
56	ADR3/	
57	ADR0/	
58	ADR1/	
59	DATE/	
60	DATF/	
61	DATC/	
62	DATD/	
63	DATA/	
64	DATB/	
65	DAT8/	
66	DAT9/	
67	DAT6/	
68	DAT7/	
69	DAT4/	
70	DAT5/	
71	DAT2/	DATA BUS
72	DAT3/	
73	DAT0/	
74	DAT1/	
75	GND	
76	GND	Ground
77	V_{BB}	
78	V_{BB}	Source power −12 VDC
79		
80		
81	V_{CC}	
82	V_{CC}	Source power +5V
83	V_{CC}	
84	V_{CC}	
85	GND	
86	GND	Ground

APPENDIX G
BLANK DECODER CHARTS

SYSTEM ADDRESS A0-15 HEX	DECODER CIRCUIT INPUTS						CE'S								
	BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	7	6	5	4	3	2	1	0	BYTE
0 X X X	0	0	0	0	1 1	0 1									L H
1 X X X	0	0	0	1	1 1	0 1									L H
2 X X X	0	0	1	0	1 1	0 1									L H
3 X X X	0	0	1	1	1 1	0 1									L H
4 X X X	0	1	0	0	1 1	0 1									L H
5 X X X	0	1	0	1	1 1	0 1									L H
6 X X X	0	1	1	0	1 1	0 1									L H
7 X X X	0	1	1	1	1 1	0 1									L H
8 X X X	1	0	0	0	1 1	0 1									L H
9 X X X	1	0	0	1	1 1	0 1									L H
A X X X	1	0	1	0	1 1	0 1									L H
B X X X	1	0	1	1	1 1	0 1									L H
C X X X	1	1	0	0	1 1	0 1									L H
D X X X	1	1	0	1	1 1	0 1									L H
E X X X	1	1	1	0	1 1	0 1									L H
F X X X	1	1	1	1	1 1	0 1									L H
X=HEX DIGITS	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	
	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

8 BIT DATA BUS

LEAVE JUMPER J20 OPEN. (NO SHORTING PLUG)

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = K BYTES

	JUMPERS			
	PROMS: 1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

SYSTEM ADDRESS A0–15 HEX	DECODER CIRCUIT INPUTS						$\overline{CE}$'S								
	BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	7	6	5	4	3	2	1	0	BYTE
0XXX	0	0	0	0	0 1 0	0 0 1									W L H
1XXX	0	0	0	1	0 1 0	0 0 1									W L H
2XXX	0	0	1	0	0 1 0	0 0 1									W L H
3XXX	0	0	1	1	0 1 0	0 0 1									W L H
4XXX	0	1	0	0	0 1 0	0 0 1									W L H
5XXX	0	1	0	1	0 1 0	0 0 1									W L H
6XXX	0	1	1	0	0 1 0	0 0 1									W L H
7XXX	0	1	1	1	0 1 0	0 0 1									W L H
8XXX	1	0	0	0	0 1 0	0 0 1									W L H
9XXX	1	0	0	1	0 1 0	0 0 1									W L H
AXXX	1	0	1	0	0 1 0	0 0 1									W L H
BXXX	1	0	1	1	0 1 0	0 0 1									W L H
CXXX	1	1	0	0	0 1 0	0 0 1									W L H
DXXX	1	1	0	1	0 1 0	0 0 1									W L H
EXXX	1	1	1	0	0 1 0	0 0 1									W L H
FXXX	1	1	1	1	0 1 0	0 0 1									W L H
	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	
X = HEX DIGITS	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

16 BIT DATA BUS

INSTALL SHORTING PLUG AT JUMPER J20.

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = __K BYTES

	JUMPERS			
	PROMS: 1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

APPENDIX H
TEST DECODING ALGORITHMS FOR 2K X 8 MOS PROMs AT 8000H

SYSTEM ADDRESS A0-15 HEX	DECODER CIRCUIT INPUTS						$\overline{CE}$'S								
	BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	7	6	5	4	3	2	1	0	BYTE
0 X X X	0	0	0	0	1	0									L
					1	1									H
1 X X X	0	0	0	1	1	0									L
					1	1									H
2 X X X	0	0	1	0	1	0									L
					1	1									H
3 X X X	0	0	1	1	1	0									L
					1	1									H
4 X X X	0	1	0	0	1	0									L
					1	1									H
5 X X X	0	1	0	1	1	0									L
					1	1									H
6 X X X	0	1	1	0	1	0									L
					1	1									H
7 X X X	0	1	1	1	1	0									L
					1	1									H
8 X X X	1	0	0	0	1	0								0	L
					1	1							0		H
9 X X X	1	0	0	1	1	0						0			L
					1	1					0				H
A X X X	1	0	1	0	1	0				0					L
					1	1			0						H
B X X X	1	0	1	1	1	0		0							L
					1	1	0								H
C X X X	1	1	0	0	1	0									L
					1	1									H
D X X X	1	1	0	1	1	0									L
					1	1									H
E X X X	1	1	1	0	1	0									L
					1	1									H
F X X X	1	1	1	1	1	0									L
					1	1									H
X=HEX DIGITS	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	
	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

8 BIT DATA BUS

LEAVE JUMPER J20 OPEN. (NO SHORTING PLUG)

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY = 2K BYTES

	JUMPERS			
PROMS:	1-4		5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0

SYSTEM ADDRESS A0–15 HEX	DECODER CIRCUIT INPUTS						$\overline{CE}$'S								BYTE
	BAF	BAE	BAD	BAC	$\overline{BHEN}$	LA0	7	6	5	4	3	2	1	0	
0XXX	0	0	0	0	0 1 0	0 0 1									W L H
1XXX	0	0	0	1	0 1 0	0 0 1									W L H
2XXX	0	0	1	0	0 1 0	0 0 1									W L H
3XXX	0	0	1	1	0 1 0	0 0 1									W L H
4XXX	0	1	0	0	0 1 0	0 0 1									W L H
5XXX	0	1	0	1	0 1 0	0 0 1									W L H
6XXX	0	1	1	0	0 1 0	0 0 1									W L H
7XXX	0	1	1	1	0 1 0	0 0 1									W L H
8XXX	1	0	0	0	0 1 0	0 0 1							0 0	0 0	W L H
9XXX	1	0	0	1	0 1 0	0 0 1					0 0	0 0			W L H
AXXX	1	0	1	0	0 1 0	0 0 1			0 0	0 0					W L H
BXXX	1	0	1	1	0 1 0	0 0 1	0 0	0 0							W L H
CXXX	1	1	0	0	0 1 0	0 0 1									W L H
DXXX	1	1	0	1	0 1 0	0 0 1									W L H
EXXX	1	1	1	0	0 1 0	0 0 1									W L H
FXXX	1	1	1	1	0 1 0	0 0 1									W L H
	A5	A4	A3	A2	A1	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	
X = HEX DIGITS	ADDRESS INPUTS 3628A						OUTPUTS								

L = LOW BYTE
H = HIGH BYTE

0 = ENABLE
1 = DISABLE

0 = NO SHORTING PLUG
X = SHORTING PLUG INSTALLED

16 BIT DATA BUS

INSTALL SHORTING PLUG AT JUMPER J20.

INSTALL SHORTING PLUGS PER THE FOLLOWING TABLE:

DEVICE DENSITY 2K BYTES

	JUMPERS			
	PROMS: 1-4		PROMS: 5-8	
	J21	J22	J23	J24
2K	0	X	0	X
4K/8K	X	0	X	0